nexCOBOT
Open Robots & Machines

SCB100

Safety Manual

(Original Instructions)

V0.66

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www.nexcobot.com

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Revision History

Date	Version	Modifications
2024.03.25	0.66	AoU_SCB100_9 is updated. Chapter 5.15 is added. Modified Figure 3. Added DDR4 information in 5.3
2024.03.11	0.65	Modified 1.1 Purpose Modified 5.1 Modified 5.5 Digital Input and 5.6 Digital Output Modified 8 Safety Analysis Results Modified Appendix B and C.
2023.12.15	0.64	Modified 5.1 Modified 5.5 and 8.1 Modified Appendix A and B.
2023.02.07	0.63	Modified DTI description of Table 7. Modified Table 24 and Table 25 due to new updated FMEDA. Added Note in 5.5.2 for SCB100-IO (Ver.D) Modified 5.5.6 for SCB100-IO (Ver.D)
2022.11.10	0.62	Added Using Digital Inputs with enabling SCB100 test pattern control and external power description in Ch6.5.3 Modified Table 41 Modified the specification of vibration and shock
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		Added Table 17. Digital Output hardware response time Modified Table 41. Other diagnostic related GPIO pin register Modified 5.5.5 Added Figure 9. Using Digital Inputs with enabling SCB100 test pattern control Added 5.5.6 Modified Figure 12. Digital output channel test pattern Modified Table 18. Truth Table of digital output channel Modified FMEDA result of Table 24 and Table 25
2021.12.09	0.51	Modified Table 38
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2021.10.29	0.30	Added Ch6, Ch7, Ch8
2021.10.01	0.20	Added Ch3, Ch4.1,4.2,4.3, Ch5
2021.09.06	0.10	First draft version of the document (Ch1)

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1 Introduction

1.1. Purpose

This document is the Safety Manual of NexCOBOT SCB100 written in compliance with EN 61508-2:2010, Annex D and EN 61508-3:2010, Annex D.

The safety controller SCB100 is an EN 61508 Compliant Item including hardware components and software components, which are intended to be integrated into safety-related programmable electronic systems.

SCB100 is leveraging Intel Atom® x6427FE functional safety processor. The user of SCB100 needs to integrate SCB100 with other safety compliant item (e.g. OS, application specific software components) to achieve a complete safety-related programmable electronic systems.

NOTE:

All the instructions and constraints as required in this safety manual as well as the manuals as listed in chapter 1.5, must be complied with by the user, in order to achieve the required systematic capability SC 2.

NexCOBOT cannot directly provide the manuals as listed in chapter 1.5 due to NDA concerns, therefore the user of SCB100 is responsible to get these user manuals from the corresponding hardware component / IC venders.

1.2. Audience

The audience for this document is anyone who needs to understand the use of this SCB100 with Intel Atom® x6427FE functional safety processor (Elkhart Lake product) in a functional safety environment. Users include, but are not limited to:

- System integration engineers and architects
- Safety Engineers and Safety Managers
- Engineers integrating and testing the product
- Auditors and Assessors

1.3. Applied standards

Functional safety standards
EN 61508:2010 Parts 1-7

EN ISO 13849-1:2023
EN ISO 13849-2:2012
EN IEC 62061:2021
ISO 10218-1:2011, clause 5.4.2
EMC standards
IEC 61326-3-1:2017
IEC 61131-2:2017
IEC 61000-6-2:2016
IEC 61000-6-4:2018
Environmental standards
IEC 61131-2:2017

1.4. Acronyms and Terminology

Table 1. Terminology

Term	Description
1oo1	Functional safety system architecture as defined in B.3.2.2.1 of EN 61508:6
AoU	Assumption of Use
BIOS	Basic Input/Output System
Cat.3	Category 3 architecture as defined in EN ISO 13849:1 6.2.6.
CCF	Common Cause failure as defined in EN 61508:4 3.6.10.
COM port	Communication port
CRC	Cyclic Redundancy Check
DC	Diagnostic Coverage
DDR	Double Data Rate
DI	Digital Input
DO	Digital Output
DTI	Diagnostic Test Interval
ECC	Error Correcting Code

Elkhart Lake	Formerly Code Name of Intel Atom® x6000E Series Processors
EMMC	Embedded Multi Media Card
EtherCAT	Ethernet for Control Automation Technology
FMEA	Failure Modes and Effects Analysis
FMEDA	Failure Modes Effects and Diagnostic Analysis
FSoE	FailSafe over EtherCAT
FuSa	Functional Safety
FW	Firmware
HFT	Hardware Fault Tolerance
HW	Hardware
IBECC	In Band Error Correcting Code, which is provided by Intel Elkhart Lake SoC
IEC	International Electrotechnical Commission
ISI	Intel® Safety Island
ISO	International Organization for Standardization
ITSS	Interrupt Subsystem
MAC	Media Access Control Address
NMI	Non Maskable Interrupt
NOK	Non OK signal derive from Intel Safety Island
NVRAM	Non-Volatile Random Access Memory
PMC	Power Management Controller
ODCC	On Demand Cross Comparison
OS	Operating System
OSAL	Operating System Adaptation layer
OVP	Over Voltage Protection
PHY	Physical Layer
SMCL	Safety Monitor Communication Library
SC	Safety Concept
SC3	Systematic Capability 3 as defined in EN 61508:4 3.5.9.
SIL	Safety Integrity Level as defined in EN 61508:4 3.5.8

SKU	Stock Keeping Unit
SRS	Safety Requirements Specification
STL	Software Test Libraries
SW	Software
UVP	Under Voltage Protection
WL	Workload (Software application)

1.5. Reference Documents

Table 2. Reference Documents

ID	Document	REV	Document No.
[1]	Elkhart Lake Safety Manual	1.3	610115
[2]	Elkhart Lake L MCP FMEDA 1oo1 and Safety Mechanism (Diagnostic) list	1.4	615613
[3]	Elkhart Lake MCP FMEDA Cat.3, PL=d	1.4	615614
[4]	Elkhart Lake Functional Safety User Guide	1.0.4	610113
[5]	14_SCB100 component level FMEA_2022-04-29_Using_Intel_New_FMEDA_2023_10-02.xlsx	0.6	14
[6]	38_SCB100_Hardware Software Interfaces Specification_V0.2_2023-1101.xlsx	0.2	38
[7]	Super I/O user manual (NCT6122D / NCT6126D Nuvoton Super I/O)	1.4	NCT6122D / NCT6126D
[8]	PCIe to EtherCAT slave controller user guide (AX99100 PCIe to Multi I/O Controller)	0.24	AX99100 V0.24/06/06/16
[9]	EtherCAT slave controller user guide (AX58100 EtherCAT slave controller)	1.2	AX58100 V1.02/11/07/18
[10]	Intel I225 Ethernet controller user guide	1.92	I225

[11]	MARVELL PHY user guide	Feb. 24, 2012	MV-S107146-00

2 Document Scope

2.1. Prerequisite Documents

It is assumed that the reader is familiar with Functional Safety and main functional safety standards, i.e.:

- EN 61508:2010, Parts 1-7
  Functional safety of electrical/electronic/programmable electronic safety related systems
- EN ISO 13849-1:2023
  Safety of machinery - Safety-related parts of control systems

Note:

The user of SCB100 must be sufficiently trained by NexCOBOT.

2.2. In Scope

Specifically:

- An overview of the assumed use cases, safety functions and safety requirements
- An overview of the diagnostic measures for which diagnostic coverage is claimed
- Assumption of Use with respect to its intended use

2.3. Out of Scope

Descriptions and guidance on how to use Intel Safety SW libraries (e.g. STL, ODCC) for user own safety SW applications is out of scope of this document.

Information on them can be found in [1] and [4].

2.4. SCB100 version

This safety manual is applied the SCB100 version as following.

Module name	HW Rev.	SW Rev.
SCB100 main board	F	File name: sbl_ifwi_ehl.bin MD5:371bbbe4fe79199337186dfcca7dcaf7 It contains the SW components as listed in Table 4
SCB100 IO board	D	-/-

3 Functional safety features of SCB100

3.1. Use case and intended application

The general use case of SCB100 is to integrate SCB100 into a safety controller system, where the safety functions of safety controller system are e.g.:

- Receive inputs through hardware-cabling of input devices (e.g. emergency stop button, light curtain, etc.)
- Receive input through safety Ethernet or safety EtherCAT of input devices (e.g. safety servo drive, safety teach pendant, safety digital remote I/O, etc.)
- Process input received from input devices as demanded by safety application software
- Transmit processed data to output devices through hardware-cabling or safety Ethernet

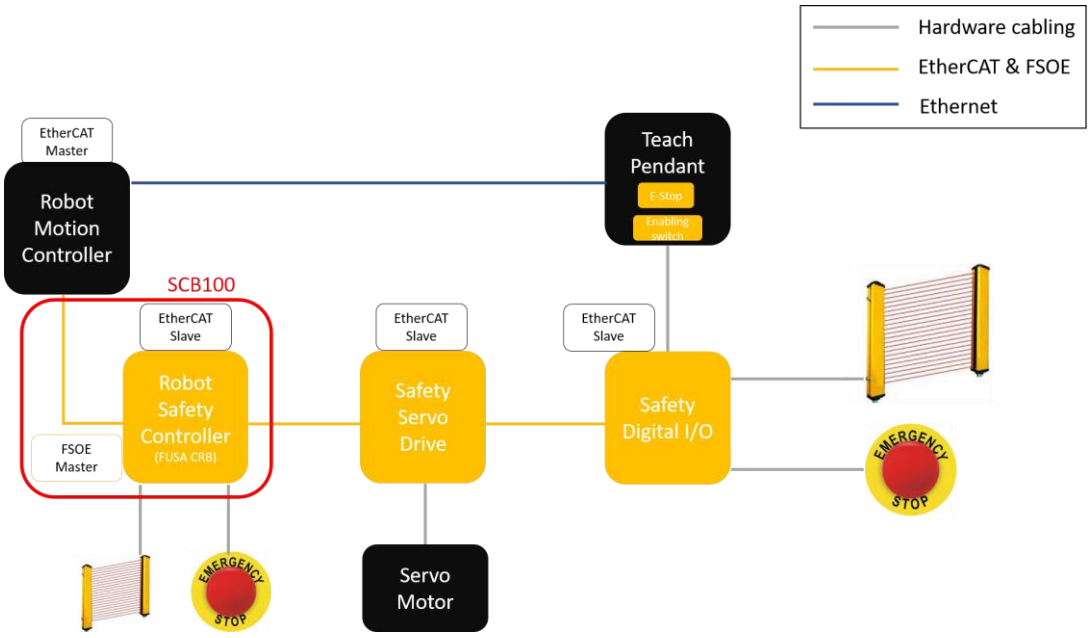


Figure 1. User scenario of SCB100

3.2. Safe function

Safety controller system (where SCB100 is integrated) will perform a logic control receiving inputs, processing them and transmitting outputs in high demand or continuous mode of operation.

Misbehavior of Safety controller system causing wrong, delayed, omitted or committed action (receive input, processing and transmit outputs) including permanent deviation in performance shall be detected and reported.

3.3. Safe state

Safe state is de-energized state.

Demand state is de-energized state.

Normal state is energized state.

3.4. Mode of operation

High demand or continuous mode.

3.5. System response time

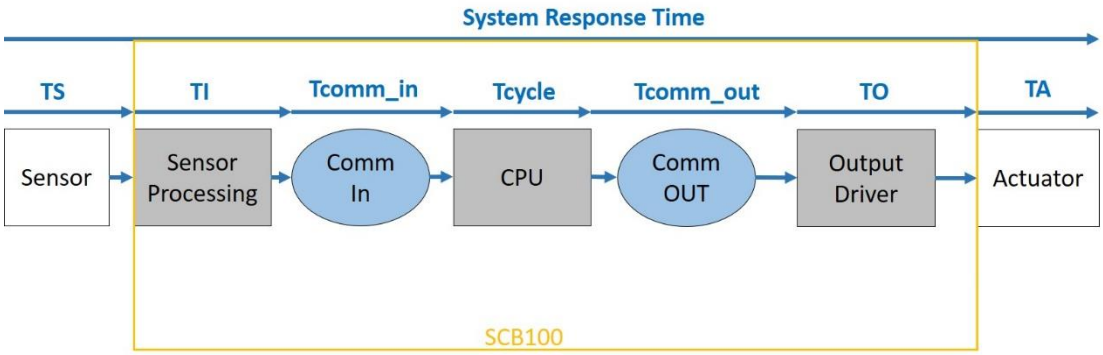


Figure 2. System Response time of SCB100

Where:

- **TS**: Reaction time required by the selected sensor to react to a process event (device specific, out of scope of SCB100)
- **TI**: The time required by the input module to sample and confirm a sensor event
- **Tcomm_in**: Input communication delay. It is equals to the sum of the time to sample a safety input module + the time required to transfer the input value to the CPU

- **TCycle**: The time which passes between a signal is received by CPU and the output is send from CPU (Including CPU processing safety SW application)
- **Tcomm_out**: Output communication delay. It is equals to the sum of the time the time required to transfer the output value from the CPU to the output module + the time to write to a safety output module
- **TO**: The time **TO** for the Safety output module is equal to the time taken by the module to react to input from controller
- **TA**: Reaction time for the selected actuator (device specific, out of scope of SCB100)

The System Response Time of Digital input and Digital outputs:

TS: given by the user of SCB100

TI + Tcomm_in: 2 ms (this is a more conservative value, for more precise values please refer to chapter 5.5.3)

TCycle: depends on SW application implemented by the user of SCB100

TO + Tcomm_out: 2 ms (this is a more conservative value, for more precise values please refer to chapter 5.6.3)

TA: given by the user of SCB100

3.6. Safety related parameters

EN 61508 parameters	
Type	B
SIL	2
SC	2
HFT (1oo1 parts)	0
HFT (1oo2 parts)	1
SFF (1oo1 parts)	> 90%
SFF (1oo2 parts)	> 60%
DTI (1oo1 parts)	See Table 7, Table 8, Table 9, Table 10, Table 19, Table 20
DTI (1oo2 parts)	< 24 hours, See Table 11, Table 15

PFH	6.103E-08 (at PTI = 20 years / MTTR=MRT=24 hours, 6.1% of SIL2)
EN ISO 13849-1 parameters	
PL	d
Category	3
DCavg	> 99%
MTTFd	See Table 25
Mission Time	< 20 years
PFH_d	1.30E-08 (at PTI = 20 years / MTTR=MRT=24 hours)

3.7. Requirements to achieve PL d / Cat. 3

In order to achieve PL d / Cat. 3, all the requirements as specified in chapter 9 of Intel Elkhart Lake Safety Manual [1] (e.g. dual redundant logical channel, etc.) must be considered by the user of SCB100.

4 Safety Architecture

4.1. SCB100 hardware block diagram

Detailed function block diagram of SCB100 can refer Figure 3.

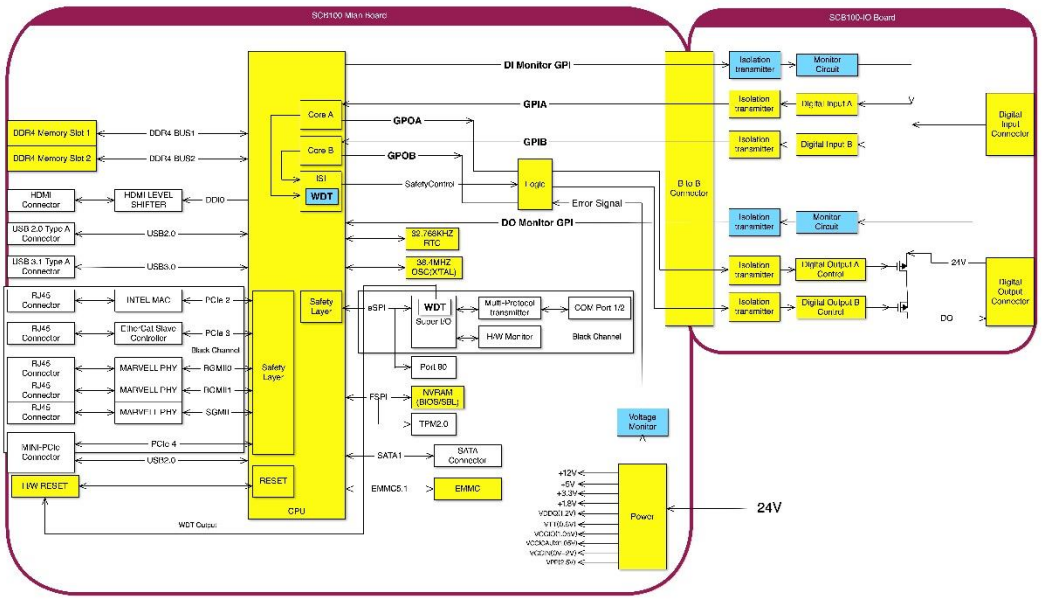


Figure 3. SCB100 Hardware block diagram

SCB100 has been partitioned in three separate sets of internal elements, with focus on their relevance for functional safety.

In Figure 3, the SCB100 blocks are identified with different colors by using the following protocol:

- **Yellow** = Safety related
- **Yellow with "Safety Layer"** = Safety related, Black channel
- **White** = Not safety related
- **Blue** = Diagnostic related

Table 3. HW elements safety classifications

H/W Element Name	Safety Classification
CPU	YES
POWER	YES
CLOCK(32.768KHZ RTC,38.4MHZ OSC)	YES

DDR4 MEMORY	YES
Intel MAC (Ethernet)	YES (black channel)
Marvell PHY (Ethernet)	YES (black channel)
USB2.0	NO
USB3.0	NO
HDMI	NO
Digital inputs	YES
Digital outputs	YES
EtherCAT	YES (black channel)
EMMC	YES
COM Port	YES (black channel)
NVRAM (BIOS/SBL)	YES
HW Reset (Include CPU Reset)	Yes

4.2. SCB100 software/firmware block diagram

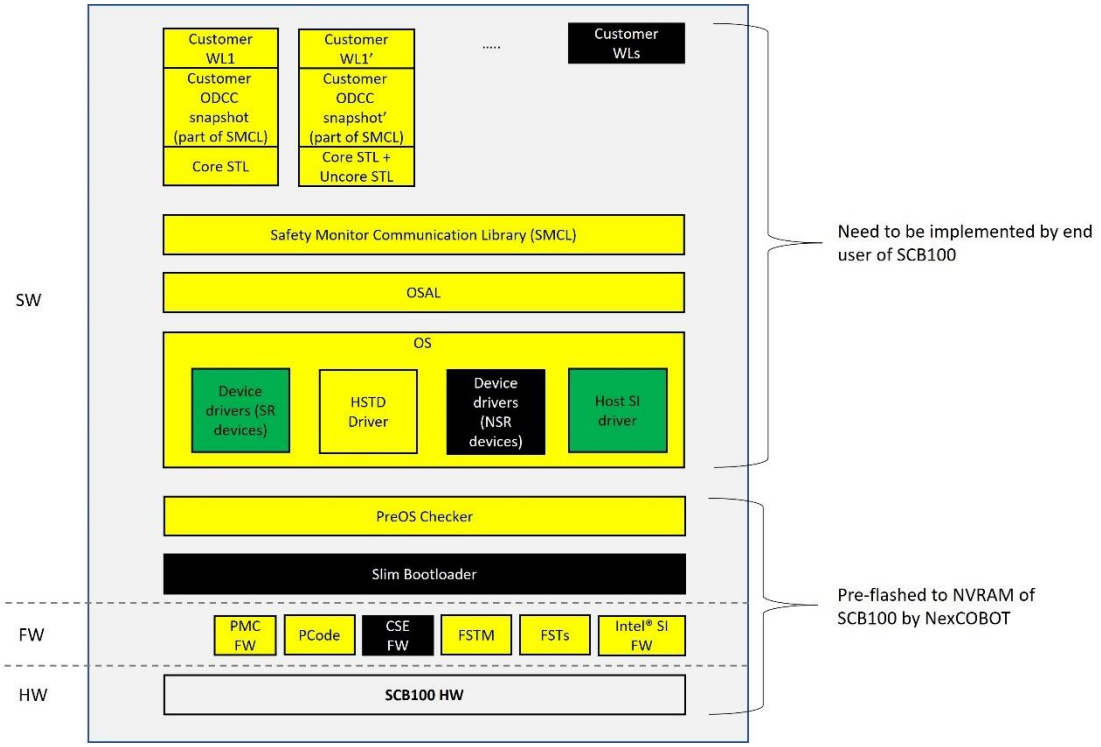


Figure 4. SCB100 Software block diagram

- **Yellow** = Safety related
- **Green** = Black channel

• **Black** = Not safety related

The software/firmware elements in Table 4 are pre-flashed into SCB100 NVRAM and are provided with SCB100 HW together to end user. If users need to modified SBL, users need to contact NexCOBOT to request to modify SBL.

Table 4. software/firmware elements safety classifications (Delivery with SCB100 HW)

software/firmware Element Name	Safety Classification	Note
Intel® SI FW	YES	FSTM (Functional Safety test Manager) and FSTs (Functional Safety Tests) are two of major components of Intel SI FW. (Refer to 6.6.2 of [1]). Intel SI FW provides measures to detect systematic faults of software components PMC FW and PCode.
FSTs	YES	
FSTM	YES	
Pre-OS Checker	YES	
PMC FW	YES	PMC FW is developed as QM software, its systematic faults are detected by Intel SI FW.
PCode	YES	PCode FW is developed as QM software, its systematic faults are detected by Intel SI FW.
Slimboot loader (SBL)	YES	Modified version for SCB100 only Slim bootloader (SBL) is developed as QM software, its systematic faults are detected by Pre-OS Checker (POSC).
CSE FW	NO	

The SW elements in Table 5 are assumed to be implemented by end user of SCB100, for the detail implementation guidance of these SW elements, please refer to Intel documents which could be found in [1] and [4].

Table 5. SW elements safety classifications (Implemented by end user of SCB100)

SW Element Name	Safety Classification	Note
OS	YES	Refer to 3.7.1 of [1]
Host SI driver	YES (Black channel)	
Device drivers (NSR devices)	NO	
Host STL Driver (HSTD)	YES	
Device drivers (SR devices)	YES (Black channel)	
OSAL	YES	Refer to 3.7.6 of [1]
SMCL	YES	Refer to 3.7.5 of [1]
STL	YES	Refer to 3.7.8 of [1]
Customer WL	YES	If the WL is used as a safety application, then this WL is safety related.

4.3. Operating States

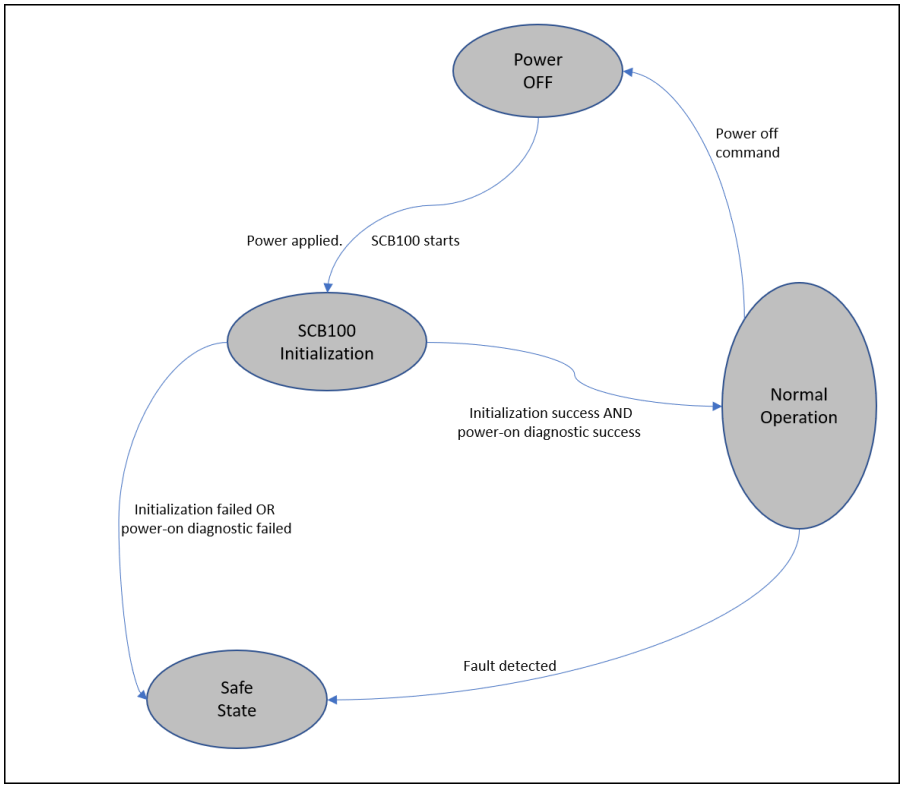


Figure 5. SCB100 State Machine

Table 6. SCB100 operating states

State	Description
Power off State	No Power applied to SCB100. All DO output OFF state
SCB100 initialization	This state covers initialization of serval components of SCB100, until Elkhart Lake SoC is ready to execute the safety function. ● Elkhart Lake IP (hardware and firmware) initialization ● Intel® Slim bootloader and pre-OS checker execution ● Super I/O initialization ● PCIe initialization ● GPIO initialization ● Memory initialization ● LAN controller and PHY initialization ● EtherCAT Salve Controller initialization ● OS download and initialization ● Initialization of all software components necessary to support Elkhart Lake functionalities and diagnostic measures ● Execution and passing of start-up STLs ● Power on diagnostic (include all functional block e.g. CPU, DI/DO circuit, etc.) ● All DO output OFF state
Normal Operation	This is the state where the safety application software is being executed. Output: depends on specific application software
Safe state	When any fault detected, SCB100 will enter safe state. e.g. all DO output OFF state.

5 Diagnostic Measures

5.1. CPU

The Intel Atom® x6427FE CPU supported by SCB100 and is compliant item developed according to EN 61508:2010 targeting a Safety Integrity level up to SIL2.

The Intel Atom® x6427FE CPU supported by SCB100 is also targeted to be compliant with EN ISO 13849 up to Cat. 3, PL d requirements.

Table 7. Diagnostic methods of CPU

Object	Diagnostics (Normal operation)	DTI / DC	Diagnostics (power-on)	Fault reaction
CPU	AoU_SCB100_1 AoU_SCB100_2 The diagnostic measures provided by Intel Atom® x6427FE processor are categorized as: Hardware: Measures which are implemented in silicon or MCP package. Typical measures include parity, ECC, CRC etc. Details provided in section 6.1 in [1]. Software: Measures which are implemented in FW component or in SW running in Intel Atom®	- DTI DTI value is defined by how user implement their software application with Intel STL (refer to section 6 in [1]) (1) SIL2, 1oo1 DC: 99.48% (Refer to Ch.10.5.2 in [1].)	According to CoU_EXT_INT_10 in Table 21 in [1], SCB100 provides the power-on diagnostic measures which are listed in Table 8.	When CPU detect faults, ISI of CPU will output safety control (NOK) signal to Logic in Figure 3, and SCB100 will enter safe state.

	processor cores. Details are provided in section 6.4. in [1].	(2) PLd, Cat.3 DCavg: 99.48% (Refer to Ch.10.6.3 in [1].)		

5.2. Power

SCB100 power input port shall be powered by the SELV/PELV power supply with a voltage range of [+24VDC-15%, 24VDC+20%] (i.e. 20.4VDC ~ 28.8VDC) to meet IEC 61131-2 standard.

Table 8. Diagnostic method of Power

Object	Diagnostics (Normal operation)	DTI / DC	Diagnostics (power-on)	Fault reaction
+24V	UVP and OVP Monitor UVP min range: 19.2V OVP max range: 28.8V (max. withstand voltage: 60V DC)	- Continuous, <2ms - DC = 99%	The same as normal operation.	When detect power has faults, the Voltage Monitor diagnostic function in Figure 3 will output Error Signal to Logic, and SCB100 will enter safe state.
12VSB	UVP and OVP Monitor OVP monitor : max : 12.6V UVP monitor : min : 11.4V (max. withstand voltage: 28.8V DC)	- Continuous, <2ms - DC = 99%	The same as normal operation.	

5VSB	UVP and OVP Monitor OVP monitor : max : 5.25V UVP monitor : min : 4.75V (max. withstand voltage: 12V DC)	- Continuous, <2ms - DC = 99%	The same as normal operation.	
3VSB	UVP and OVP Monitor OVP monitor : max : 3.46V UVP monitor : min : 3.15V (max. withstand voltage: 12V DC)	- Continuous, <2ms - DC = 99%	The same as normal operation.	
1.8VSB	UVP and OVP Monitor UVP and OVP Monitor OVP monitor : Max : 1.9V UVP monitor : min : 1.7V (max. withstand voltage: 12V DC)	- Continuous, <2ms - DC = 99%	The same as normal operation	
VPP(2.5V)	UVP and OVP Monitor OVP monitor : Max : 2.62V UVP monitor : min : 2.38V (max. withstand voltage: 12V DC)	- Continuous, <2ms - DC = 99%	The same as normal operation	
VDDQ(1.2V)	UVP and OVP Monitor OVP monitor : Max : 1.26V	Continuous, <2ms - DC = 99%	The same as normal operation	

	UVP monitor : min : 1.15V (max. withstand voltage: 12V DC)			
VTT(0.6V)	UVP and OVP Monitor OVP monitor : Max : 0.64V UVP monitor : min : 0.565V (max. withstand voltage: 12V DC)	Continuous, <2ms - DC = 99%	The same as normal operation	
VCCIO(1.05V)	UVP and OVP Monitor OVP monitor : Max : 1.1V UVP monitor : min : 1V (max. withstand voltage: 12V DC)	Continuous, <2ms - DC = 99%	The same as normal operation	
VCCINAUX(1.8V)	UVP and OVP Monitor OVP monitor : Max : 1.9V UVP monitor : min : 0.7V (max. withstand voltage: 12V DC)	Continuous, <2ms - DC = 99%	The same as normal operation	
VCCIN(0.7V-2V)	UVP and OVP Monitor OVP monitor : Max : 2.1V UVP monitor : min : 0.7V (max. withstand voltage: 12V DC)	Continuous, <2ms - DC = 99%	The same as normal operation	

5.3. DDR4 Memory

The SCB100 supports two external DDR4 SO-DIMM memory (Innodisk DDR4 3200 SO-DIMM 16G), maximum memory range can up to 32GB. The function of memory is used for when the user of SCB100 implement their own software applications, memory gives these software applications a place to store and access data on a short-term basis.

Table 9. Diagnostic methods of Memory

Object	Diagnostics (Normal operation)	DTI / DC	Diagnostics (power-on)	Fault reaction
Memory (DDR)	AoU_SCB100_4 **(1) HW IBECC** SCB100 protects selected memory regions with IBECC mechanisms detecting two bit faults and correcting single bit faults. Also, IBECC can detect address line fault. (IBECC was provided by Intel Atom® x6427FE Processor, refer to Table 16. in [1], also refer to [3] Tab/Sheet: Safety Mechanisms_Cat3Pld ID: PACKAGE_SMA17 **(2) SW ODCC** (Need to implement by the user of SCB100, AoU_SCB100_2)	- DTI (1) HW IBECC: Continuous, always active diagnostic faults in DRAM are detected by IBECC when the data is used, i.e. when RAM is read (2) SW ODCC Continuous, safety loop period (the user of SCB100 parameter)	The same as normal operation.	**Single bit error** When IBECC corrects a single bit error, it generates NMI via ITSS . NMI handler reads IBECC error status registers and report to file system. Every DTI an STL reads the file system and reports a correctable error to ISI. ISI drives ALERT_N and does required correctable error handling tasks. **Double bits error** When IBECC detects a double bits error (uncorrectable) it generates NMI via ITSS . NMI handler

	SW ODCC identifies delayed execution, wrong execution, stall and wrong memory management in Core by running safety application in two (or more) independent cores and sending ODCC snapshots to ISI. If comparison between the ODCC snapshots fail, ISI will drive “NOK “. (Refer to Table 19. in [1])	- DC = 99%		reads IBECC error status registers and report to file system. An STL reads the file system and report uncorrectable error to ISI. ISI drives NOK (Safety Control) to Logic function of SCB100 in Figure 3, and SCB100 will enter safe state.

5.4. EMMC

The SCB100 supports one storage device EMMC. EMMC is the hardware component that stores all of digital content, such as documents, pictures, music, videos, programs, application preferences, and operating system represent digital content stored on storage.

Table 10. Diagnostic methods of EMMC

Object	**Diagnostics (Normal operation)**	**DTI / DC**	**Diagnostics (power-on)**	***Fault reaction***
Storage (eMMC)	AoU_SCB100_5 (1) CRC (Need to implement by the user of SCB100, refer to Table 21. conditions of use in [1], ID: CoU_EXT_INT_04)	DTI: No DTI as CRC and TIMEOUT are not periodic diagnostic. (Faults in external storage are detected	The same as normal operation.	Since the diagnostics of storage was implemented by the user of SCB100, the user of SCB100 need to decide what kind of fault reaction need to do when detect storage fault.

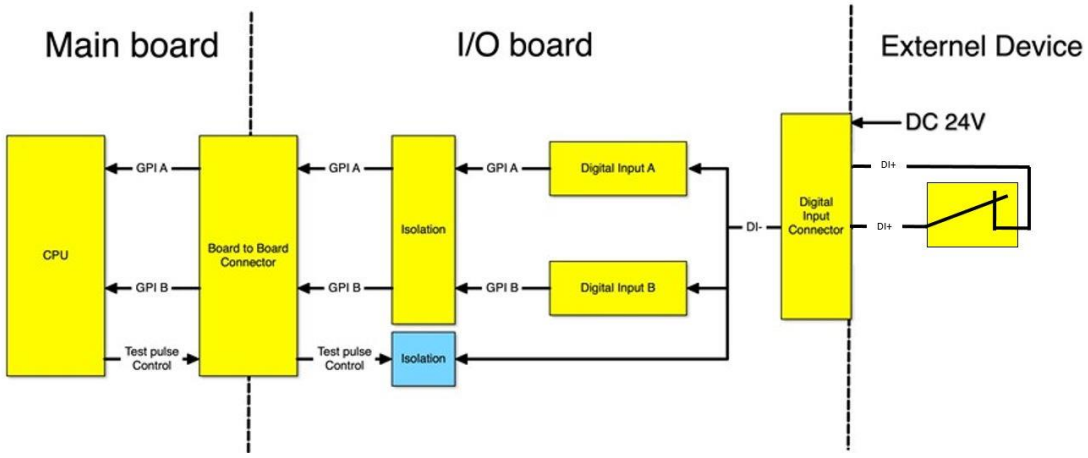
	CRC identifies data corruption and stall in eMMC by generating CRC7 for commands and CRC16 for data by CRC generators and checks present in eMMC controller. (2) TIMEOUT (Need to implement by the user of SCB100, refer to Table 21. conditions of use in [1], ID: CoU_EXT_INT_04) the timeout mechanism is implemented to protect memory accesses.	when the data is used, i.e. when eMMC is read. DC = 99%		

5.5. Digital Input

5.5.1. Function and diagnostic measures

The digital inputs of the SCB100 can detect changes in logic states for each input channel. They are capable of detecting input devices such as normally closed (NC) devices or output signal switching devices (OSSD). If a voltage exceeds or falls below a specific threshold, the SCB100 registers the digital input accordingly. For voltages exceeding 11VDC, the SCB100 detects the digital input as high/1. Conversely, if the voltage drops below 5VDC, the SCB100 identifies the digital input as low/0.

Additionally, each DI channel features a built-in hardware low-pass filter designed to filter out pulse signals shorter than 350μs.



Yellow = Safety related

Blue = Diagnostic related

Figure 6. Digital inputs block diagram

Table 11. Diagnostic methods of digital inputs

Object	Diagnostics (Normal operation)	DTI / DC	Diagnostics (power-on)	Fault reaction
Digital Input	AoU_SCB100_6 **Digital Input Anti-Valant design** The digital input has an Anti-Valant design, the combination of 2 channel of input signal is listed in Table 12.	- DTI Continuous, DTI value is defined by software application - DC = 99%	The same as normal operation.	When the input signal of DIA/DIB is 0/0 or 1/1, indicating a fault in the input, the CPU GPI can read the input signal of DIA/DIB. Users of the SCB100 need to develop their own software application to manage this input fault.
	Over Voltage Protection The SCB100 contains overvoltage detection chipset that can detect overvoltage on the digital input channels.	- DTI Continuous, <100ms - DC = 99%	The same as normal operation.	When the input voltage exceeds DC 30V, the overvoltage chipset will enter to fault mode with latency 25μs. In fault mode, the overvoltage chipset reduces the input current limitation to 3mA,and the corresponding output channel is deactivated.
	AoU_SCB100_7 **Test pattern** Each DI channel has a built-in hardware low-pass filter capable of filtering out pulse signals under 350μs from NC devices or OSSD devices. Users of the SCB100 can enable test pattern function via the	- DTI Continuous, DTI value is defined by software application	The same as normal operation.	The user of the SCB100 shall execute the test pattern software application on the DI. Upon detecting any fault, the test pattern software

	DI Test Pulse Control pin, allowing the system to verify that the DI port is still functioning correctly. (See 5.5.4)	- DC = 99%		shall activate ISI NOK to drive the SCB100 to enter a safe state
	Power Input Monitor The SCB100 is equipped with overvoltage protection (OVP) and undervoltage protection (UVP) monitors for the +24V power input. The voltage limits are set between 28.8V and 20.4V (max. withstand voltage: 60V DC)	- DTI Continuous, <100ms - DC = 99%	The same as normal operation.	When the +24V input voltage exceeds the overvoltage limit or falls below the undervoltage limit, the "Voltage Monitor" will cut off the power output to "DI+" to force "DI-" low. Consequently, the related digital input channels will enter a safe state. Users of SCB100 could then implement their own software application to handle this type of fault by reading the "GPIA/GPIB/GPIC Voltage Monitor" Pin (Refer to Table 41).

Table 12. Anti-valent design for DI- channel

DI- channel status	GPIA	GPIB
DI- signal is high	1	0
DI- signal is low	0	1
DI- channel has fault	1	1
DI- channel has fault	0	0

5.5.2. **Faults and fault exclusion of external wiring**

The following fault exclusion measures against wiring faults must be implemented by the user/integrator at application level.

(1) Open circuit of wiring

The safety sensor connected to DI is assumed to use in normally closed mode.

If the circuit of wiring is opened, this situation is failed safe.

(2) Short circuit of power supply, Short circuit to GND, Short circuit to other DI channels

According to ISO 13849-2:2012 Annex D Table D.4:

Short circuits between conductors which are

- permanently connected (fixed) and protected against external damage, e.g. by cable ducting, armouring,
- separate multicore cables,
- within an electrical enclosure (see remark),or individually shielded with earth connection.

5.5.3. **Digital Inputs hardware response time**

The hardware response time of digital input from 「DI-」 to 「GPIA/B of CPU」 is listed in Table 13.

Table 13. Digital inputs hardware response time

SCB100-IO: Ver.D 40CA

Signal transitioning from Low to High	Signal transitioning from High to Low
86.22us	930us

In Figure 9, when DI receives a low voltage signal from user input, it filters out low voltage signals with a duration less than 930 us. This includes the 350 us from the hardware filter and the response time of the digital input circuit.

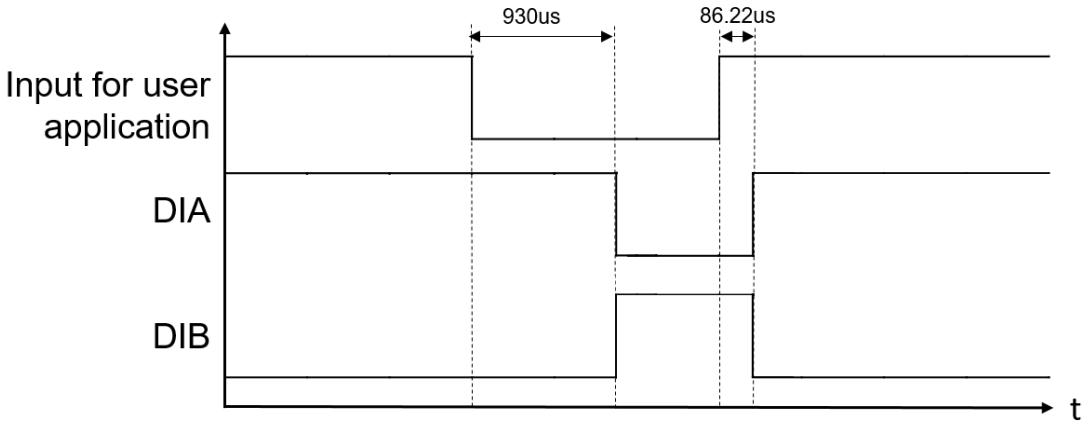


Figure 7.Digital input hardware response time waveform

5.5.4. **Digital Input channel with test pattern**

Figure 8 shows an example of applying a test pattern to a digital input channel. Users of SCB100 shall develop a software application to control the ‘Test Pulse Control' GPO (refer to Table 39 for test pulse control) to detect the failure of each digital input channel. Table 14 shows the truth table of digital input channel with test pattern.

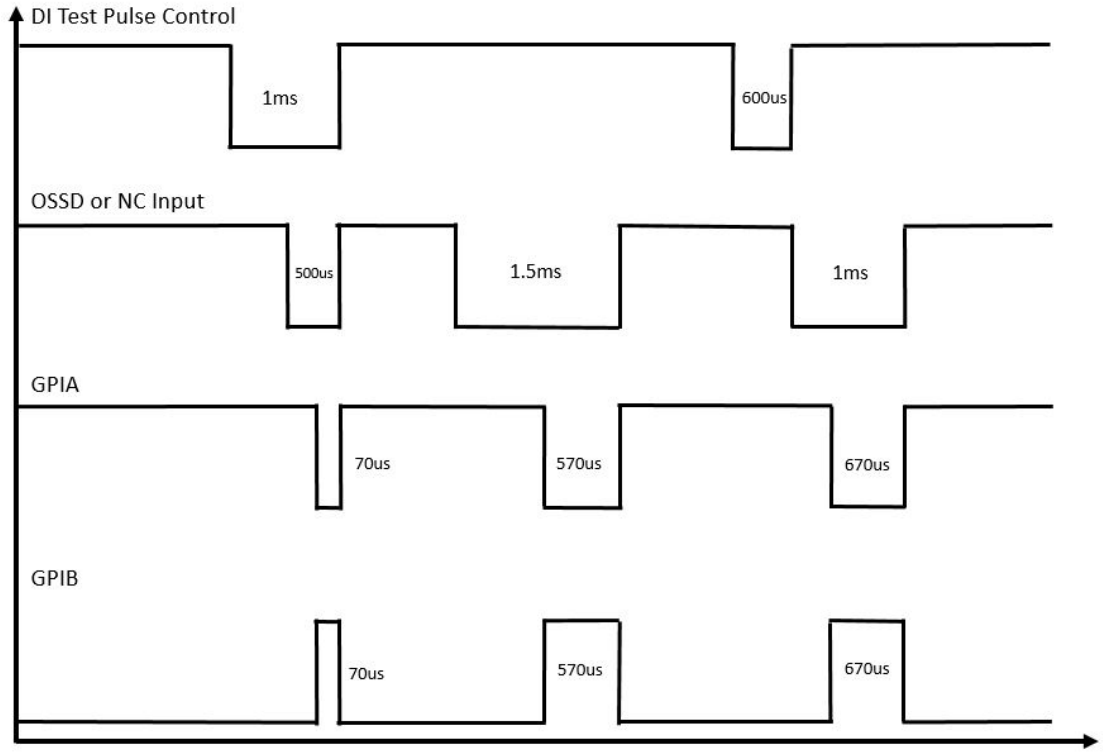


Figure 8.Digital input channel with test pattern example

Table 14. Truth table of digital input channel with test pattern

Signal	Status	Status	Status
DI Monitor Control	0	1 (>350μs)	0
(OSSD & NC Input) D1-	1	1	0 (>350μs)
GPIA	1	0	0
GPIB	0	1	1

5.5.5. **Connect** a normally closed (NC) device to the digital inputs

Figure 9 shows the wiring example for connecting SCB100 digital inputs to a safety switch device (e.g., E-Stop button, enabling switch) and enabling test pattern control of SCB100. Users need to use the DI+ channel to output a high voltage to the safety switch device input, and then connect the safety switch device output back to the DI- channel.

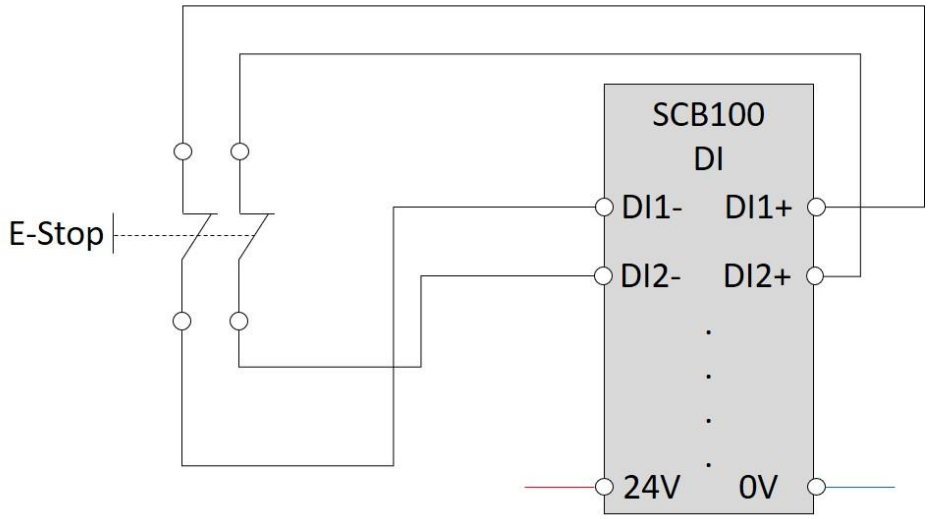


Figure 9. Using Digital Inputs with enabling SCB100 test pattern control

Note:

For the requirements of fault exclusion measures against wiring faults, refer to chapter 5.5.2.

5.5.6. **Connect an Output Signal Switching Device (OSSD) to the digital input ports**

Figure 10 shows the wiring example for connecting SCB100 digital inputs to a safety sensor device with OSSD outputs (e.g., Light curtain). In this scenario, users SHALL NOT use DI+ to provide power to the safety sensor device. Instead, they shall use external 24V power for the safety sensor device.

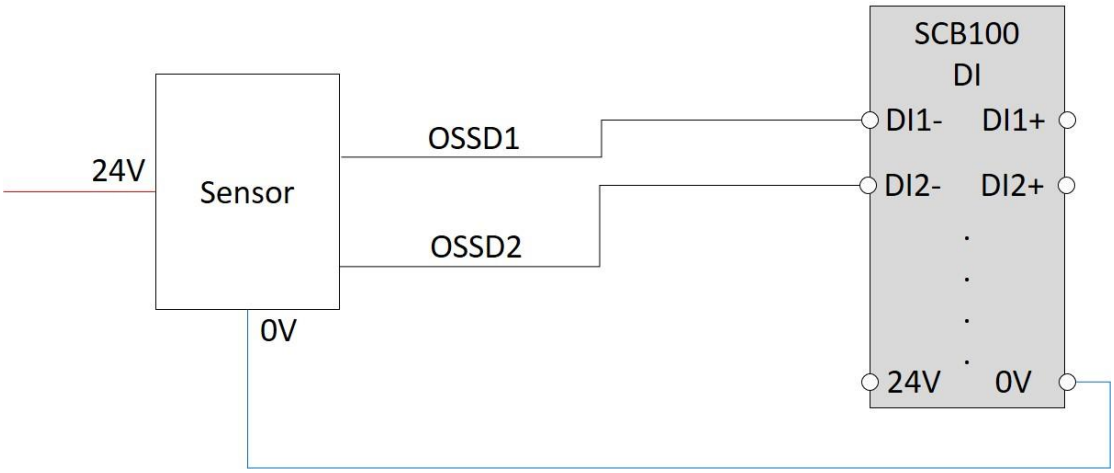


Figure 10. Using Digital Inputs without enabling SCB100 test pattern control

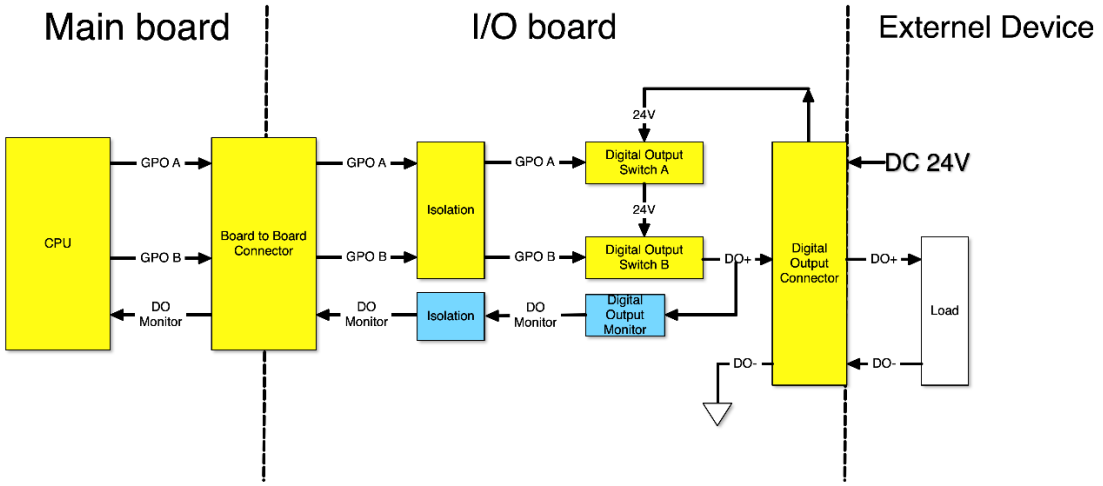
Note:

For the requirements of fault exclusion measures against wiring faults, refer to chapter 5.5.2.

5.6. Digital Output

5.6.1. Function and diagnostic measures

Digital Outputs on the SCB100 can generate logic states for each output channel. They enable users to control voltage using their software application. When the software application commands the output to be high, it generates a voltage. Conversely, when the software application commands the output to be low, it is connected to ground and does not produce any voltage. Additionally, digital outputs feature an Anti-Valent design, as demonstrated in Table 16.



Yellow = Safety related

Blue = Diagnostic related

Figure 11. Digital outputs block diagram

Table 15. Diagnostic methods of digital outputs

Object	Diagnostics (Normal operation)	DTI / DC	Diagnostics (power-on)	Fault reaction
Digital Output	AoU_SCB100_8 **Test pattern – "Dark Test"** The user of SCB100 shall implement SW application to diagnose the switch-off capability of each MOFET using the test pattern – "Dark Test" as shown in Figure 12 and Table 18: • If the DO+ output voltage is under 3V, the DO monitor will read back as logic LOW. • If the DO+ output voltage is a little	- DTI **Test pattern** Continuous, DTI value is defined by software application - DC = 99%	The same as normal operation.	The user of SCB100 shall execute test pattern SW application to DO. When any fault detected, the test pattern software shall drive ISI NOK to let SCB100 enter safe state.

	higher than 3V, the DO monitor will read back as logic HIGH, meaning not real switched off or de-energized.			
	Output over current protection: Each DO have an external FUSE to protection over current	- DTI **Output over current protection:** Continuous, <100ms - DC = 99%	The same as normal operation.	When the +24V input voltage exceeds the overvoltage limit, falls below the undervoltage limit, or exceeds the current limit, the "Voltage Monitor" will deactivate the power output to "DO+" and the related digital output (DO) channels will enter a safe state. Users of the SCB100 can monitor the fault state through the " GPO Voltage Monitor " pin (refer to Table 41) and develop their own software application to
	Power Input monitor: The SCB100 is equipped with overvoltage protection (OVP) and undervoltage protection (UVP) monitors for the +24V power input. The voltage limits are set between 28.8V and 20.4V (max. withstand voltage: 60V DC)	- DTI **Power Input monitor** Continuous, <100ms - DC = 99%	The same as normal operation.	

				manage this type of fault.

Table 16. Anti-valent design for DO+ channel

DI- channel status	GPOA	GPOB
DO+ signal is high	1	0
DO+ signal is low	0	1
DO+ signal is low	1	1
DO+ signal is low	0	0

5.6.2. **Faults and fault exclusion of external wiring**

The following fault exclusion measures against wiring faults must be implemented by the user/integrator at application level.

(1) Open circuit of wiring

None. (No influence to output device)

(2) Short circuit of power supply and short circuit to GND

According to ISO 13849-2:2012 Annex D Table D.4:

Short circuits between conductor and any exposed conductive part within an electrical

Enclosure. Provided both the conductors and enclosure meet the appropriate requirements (see IEC 60204-1:2016).

(3) Short circuit to other DO channels

According to ISO 13849-2:2012 Annex D Table D.4:

Short circuits between conductors which are

- permanently connected (fixed) and protected against external damage, e.g. by cable ducting, armouring,
- separate multicore cables,
- within an electrical enclosure (see remark),or
- individually shielded with earth connection.

5.6.3. **Digital Outputs hardware response time**

The hardware response time of digital input from 「GPIA/B of CPU」to「DO+」is listed as Table 17.

Table 17. Digital Output hardware response time

SCB100-IO: Ver.D 40CA	
Signal transitioning from Low to High	Signal transitioning from High to Low
13.61us	196.0us

5.6.4. **Digital Output channel with test pattern**

Figure 12 shows the example that how to control 「GPOA」and 「GPOB」to perform a test pattern to diagnose DO channel, and read the status of 「DO monitor」to check each output channel. (Refer to Table 18 for more details)

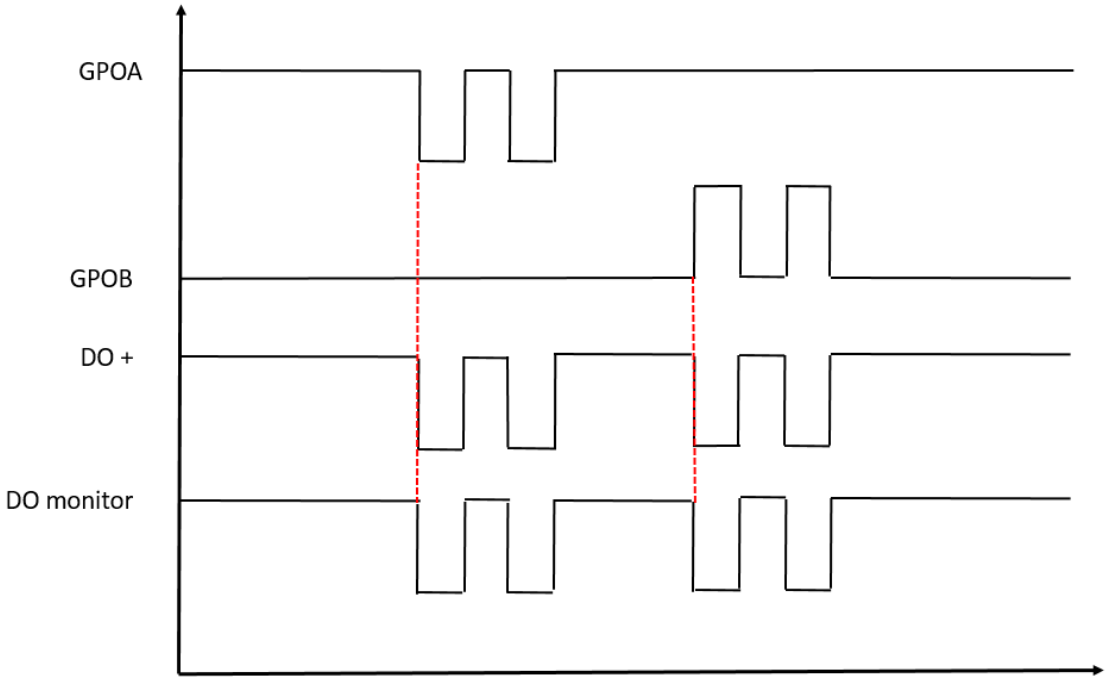


Figure 12. Digital output channel test pattern

Table 18. Truth Table of digital output channel

Signal	Status	Status	Status	Status
GPOA	1	0	1	0

GPOB	0	1	1	0
DO +	1	0	0	0
DO Monitor	1	0	0	0

5.6.5. Connect a load to the digital output ports

Figure 13 shows the wiring example for connecting SCB100 digital outputs to a load. Users need to use the DO+ channel to output a high voltage to the load, and then connect the ground voltage back to the DO- channel.

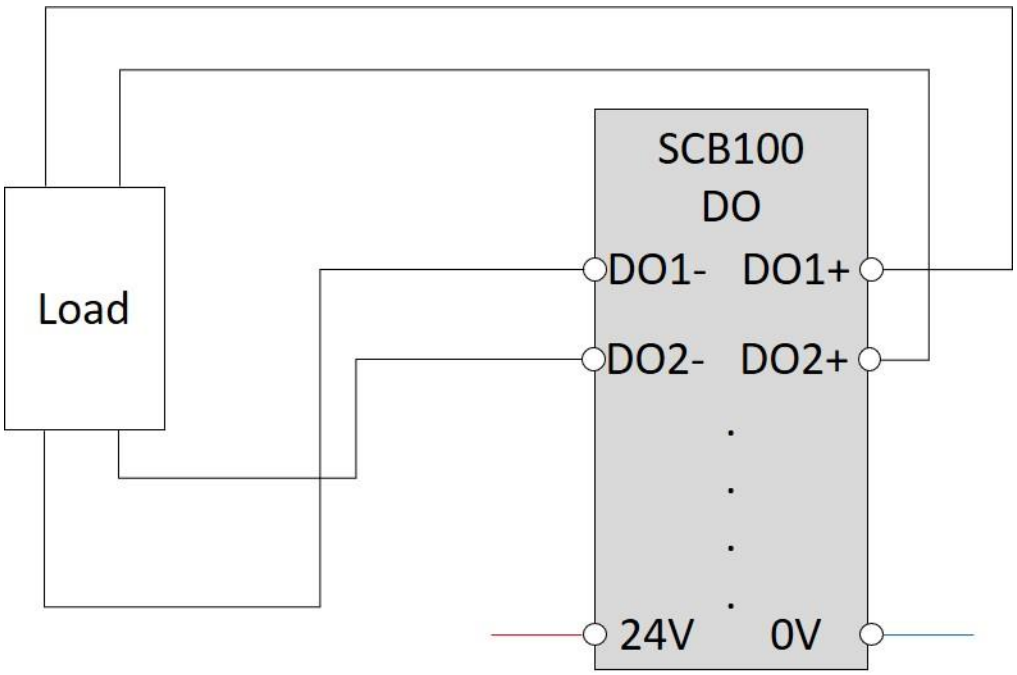


Figure 13. Connect a load to digital output ports

Note:

For the requirements of fault exclusion measures against wiring faults, refer to chapter 5.6.2.

5.7. NVRAM

The main usage of NVRAM of SCB100 is to use to store boot / BIOS image. The boot image (SBL & Pre-OS checker, see Figure 4) of SCB100 is stored in NVRAM. When SCB100 is in initializing state in Figure 5, Data regions in flash

pertaining to the Flash Descriptor region and platform initialization code shall be protected with CRC and checked by Intel Atom® x6427FE Processor during boot. After SCB100 successful boot OS, SBL and Pre-OS check won't work anymore.

In case the user use it to store safety related data e.g. application program, corresponding diagnostic measures shall be implemented by the user at application level.

Table 19. Diagnostic methods of NVRAM

Object	**Diagnostics (Normal operation)**	**DTI / DC**	**Diagnostics (power-on)**	***Fault reaction***
NVRAM	The NVRAM will not use after boot into OS (Normal operation state).	- DTI: N/A - DC = 99%	CRC to identify data corruption and stall in NVRAM (Which is provided by Intel Atom® x6427FE Processor, refer to [3], sheet "SKU11 Cat3 PLd FMEDA" Row 31.	If detect faults in initialization state, SCB100 won't enter normal operation state.

5.8. HW Reset

HW Reset is the reset circuit outside of CPU and is using to reset the whole SCB100 including CPU. This HW reset can also be used for debug purpose by the dedicated button.

If the reset circuit has faults, which means some components of SCB100 are not sufficiently reset, and there are two indirect diagnostic methods can detect the reset faults:

Fault tolerance:

See Figure 3, dual redundant reset circuitry are implemented, i.e. “H/W RESET” and CPU internal “RESET”.

AoU_SCB100_9

The user of SCB100 shall implement the “temporal and logic monitoring of program sequence” at its specific application level, which is in combine with Intel® Safety Island (works as comparator and watchdog, refer to Intel safety manual 610115 V1.3 chapter 6.4.2.1), can indirectly cover the faults of reset circuitry. When fault detected the SCB100 enter into safe state by switch-off logic in Figure 3.

Note:

The external watchdog integrated within the chip Super I/O cannot be used in safety related applications.

AoU_SCB100_10

The user of SCB100 shall implement the safety layer of communication bus i.e. EtherCAT, Ethernet, COM Port, PCIe on Mini-PCIe (see chapter 5.10 – 5.13). Those safety layers can indirectly cover the faults of reset circuitry.

5.9. Clock

There are two clocks of SCB100, which are 32KHz RTC and 38.4MHz XTALs(OSC).

Table 20. Diagnostic methods of Clock

Object	Diagnostics (Normal operation)	DTI / DC	Diagnostics (power-on)	*Fault reaction*
RTC	AoU_SCB100_11 If RTC is used for safety related time keeping purpose, the user of SCB100 needs to detect faults in time keeping by comparing with another	- DTI: Continues, safety loop period (the user of	N/A	The user of SCB100 need to drive ISI to output safety control signal to SCB100, and

	reference real time clock. (Details provided in Table 24 in [1], the diagnostic measures ID is CoU_RTC_MONITORING_01).	SCB100 parameter)		SCB100 will go into safe state.
OSC	RTC, OSC and ISI CRO are fed into a cross monitoring circuit in the ISI that detects stuck at and frequency change faults (Details provided in Table 15 in [1], the diagnostic measures ID is HW_clock_monitoring).	- DTI: Continues, <2ms - DC = 99%	N/A	ISI of CPU will derive Safety Control output to Logic to let SCB100 enter safe state.

5.10. EtherCAT Slave (Black channel)

The SCB100 has an EtherCAT Slave Controller (ESC) which can process EtherCAT frames. With this ESC, SCB100 can be an EtherCAT slave using in the EtherCAT application. The EtherCAT slave has two RJ45 connector and can receive and transmit data through these RJ45 connector. In addition, according to Figure 3, EtherCAT slave communicate with CPU through PCIe bus.

AoU_SCB100_12

EtherCAT slave can be treat as a black channel of safety related function of SCB100. If EtherCAT slave function will use to be safety function of SCB100, the user must implement sufficient diagnostic measures (e.g. Functional Safety over EtherCAT (FSoE) protocol) at application level according to standard e.g. IEC 61784-3:2021.

5.11. Ethernet (Black channel)

SCB100 provides four network ports, all of which support 10/100/1000Mbps Ethernet functionality. One of these ports utilizes the I225 Ethernet controller, capable of achieving speeds of up to 2.5G. The remaining three ports utilize the MARVELL 88E1512 PHY transmitter. These four network ports adhere to the IEEE802.3 standards.

AoU_SCB100_12

Ethernet function can be treated as a black channel of safety related function of SCB100. If Ethernet function will be used as safety function of SCB100, the user must implement sufficient diagnostic measures according to e.g. IEC 61784-3:2021.

5.12. COM port (Black channel)

The SCB100 provides two COM ports and these two ports can support RS232/422/485 protocol. The user of SCB100 can switch protocol by controlling GPIO.

AoU_SCB100_12

COM port function can be treated as a black channel of safety related function of SCB100. If COM port function will be used as safety function of SCB100, the user must implement sufficient diagnostic measures according to e.g. IEC 61784-3:2021.

5.13. Mini-PCIe (PCIe, Black Channel)

SCB100 provides one Mini-PCIe slot for the user of SCB100 to expansion functions, and this Mini-PCIe port provides one PCIe x 1 and one USB2.0.

AoU_SCB100_12

PCIe function can be treated as a black channel of safety related function of SCB100. If PCIe function will used to be safety function of SCB100, the user must implement sufficient diagnostic measures according to e.g. IEC 61784-3:2021.

5.14. USB2.0 (non-safety related)

USB2.0 is **NOT** designed to be used for safety related functions.

5.15. Safe Logic

The block “Logic” of Figure 3, is a safe logic, which is utilized to receive fault reaction signals and transition the DO output channels into a de-energized state. Its functionality and interfaces are as following:

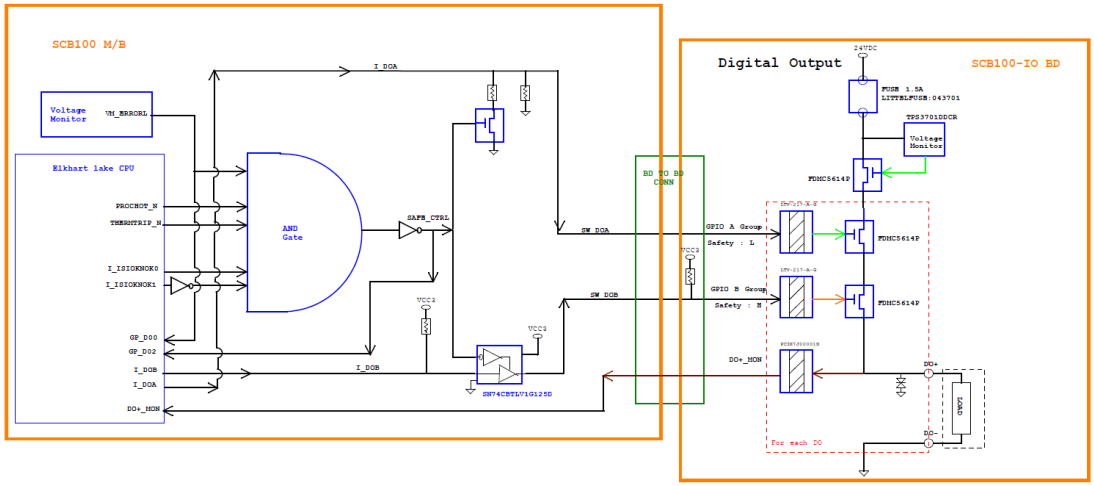


Figure 14. Detail description of safe logic block diagram

Table 21. Diagnostic methods of Clock

Signal		Status	Status
		Normal	Safe State
Input	VM_ERRORL	1	Not Logic 1
	PROCHOT_N	1	Not Logic 1
	THERMTRIP_N	1	Not Logic 1
	I_ISIOKNOK0	1	Not Logic 1
	I_ISIOKNOK1	0	Not Logic 0
Output	SAFE_CTRL	0	1
	SW_DOA	I_DOA (could be 1 or 0)	0
	SW_DOB	I_DOB(could be 1 or 0)	1

6 Assumption of Use

This section specify all the SCB100 Assumption of Use (AoUs, it is called Condition of Use (CoUs) in Intel safety manual [1]) to be satisfied in order to reach the SIL 2 and Cat. 3 / PL d.

The SCB100 Assumption of use (AoU) are derived from one among following:

- Derived from the SCB100 Safety Concept, it mainly includes assumption of use related to interfaces, system and environment constraints, configurations, safe state, SW architecture.
- Derived from Elkhart Lake Safety Manual [1] CoUs .

Table 22. AoUs of SCB100

ID	Description	Reference COU of [1]
AoU_SCB100_1	The user of SCB100 need to implement STL to detect HW random failures of Intel Atom® cores and uncores. Refer 6.4.1 of [1] for more detail information about STL.	CoU_STL_01 CoU_STL_03A CoU_STL_03B CoU_STL_03C CoU_STL_04
AoU_SCB100_2	The user of SCB100 need to implement ODCC to detect HW random failures affecting the core and some other parts. Refer 6.4.2 of [1] for more detail information about STL.	CoU_ODCC_01A CoU_ODCC_01B CoU_ODCC_02A CoU_ODCC_03 CoU_ODCC_04 CoU_ODCC_05A CoU_ODCC_05B
AoU_SCB100_3	When Power diagnostic function detect power failures, the voltage monitor block will output an error signal to logic, and SCB100 will enter safe state (refer to Figure 3). The user of SCB100 can implement SW to read specific GPI pin to get the power diagnostic result. (Refer to **C.1.3 Other diagnostic related GPIO pin register**)	CoU_EXT_INT_10

AoU_SCB100_4	DDR4 memory is protected by the HW_IBECC mechanism, and HW_IBECC is enabled by SBL. SBL is provided by NexCOBOT and pre-flashed to NVRAM. The user of SCB100 shall use the HW_IBECC mechanism by making sure that all safety related data are stored in memory regions protected by HW_IBECC	CoU_EXT_INT_07
AoU_SCB100_5	If the user of SCB100 need to use EMMC to store safety related data for safety SW applications, CRC and Timeout diagnostic measures must be implemented by user SW applications.	CoU_EXT_INT_04
AoU_SCB100_6	When the input signal of DIA/DIB is 0/0 or 1/1, indicating a fault in the input, the CPU GPI can read the input signal of DIA/DIB. Users of the SCB100 need to develop their own software application to manage this input fault.	CoU_CAT.3_07
AoU_SCB100_7	The user of SCB100 need to implement test pattern diagnostic measures to each **Digital Input** channel by user SW applications. When any fault detected, the test pattern SW shall drive ISI NOK to let SCB100 enter safe state.	CoU_EXT_INT_05b CoU_DRIVENOK/ALERT_01
AoU_SCB100_8	The user of SCB100 need to implement test pattern diagnostic measures to each **Digital output** channel by user SW applications. (Refer to 5.6.2 for more details) When any fault detected, the test pattern SW shall drive ISI NOK to let SCB100 enter safe state. (The output over current fault will be covered by test pattern diagnostic method)	CoU_EXT_INT_05b CoU_DRIVENOK/ALERT_01

AoU_SCB100_ 9	The user of SCB100 shall implement the "temporal and logic monitoring of program sequence" at its specific application level, which is in combine with Intel® Safety Island (works as comparator and watchdog, refer to Intel safety manual 610115 V1.3 chapter 6.4.2.1), can indirectly cover the faults of reset circuitry. When fault detected the SCB100 enter into safe state by switch-off logic in Figure 3. Note: The external watchdog integrated within the chip Super I/O cannot be used in safety related applications.	
AoU_SCB100_ 10	The user of SCB100 shall implement the safety layer of communication bus i.e. EtherCAT, Ethernet, COM Port, PCIe on Mini-PCIe (see chapter 5.10 – 5.13). Those safety layers can indirectly cover the faults of reset circuitry.	
AoU_SCB100_11	If RTC clock is used for safety related time keeping purpose, the user of SCB100 needs to detect faults in time keeping by comparing with another reference real time clock.	CoU_RTC_MONITORING_01 CoU_DRIVENOK/ALERT_01
AoU_SCB100_12	For using the black channel related interface, the user of SCB100 need to use black channel techniques according to EN 61508-2:2010, 7.4.11.	CoU_EXT_INT_05a CoU_DRIVENOK/ALERT_01

7 SCB100 SW Architecture Recommendations

The user of SCB100 is responsible to build safety SW components.

Figure 4 shows SW Architecture of SCB100 and list the SW components which shall be implemented by the user of SCB100.

The modified version of Intel SBL is pre-flashed into SCB100 NVRAM, the user of SCB100 won't need to prepare Intel SBL by themselves. The modified Intel SBL (integrated with POSC) is followed CoU_SWARCH_03 of [1].

Table 23. AoUs on SW Architecture of SCB100

ID	Description	Reference COU of [1]
AoU_SCB100_SW_1	The user of SCB100 shall select a proper OS (and hypervisor if used to a virtualized environment) according to the system level safety requirements on which to implement their applications.	CoU_SWARCH_01 CoU_SWARCH_02
AoU_SCB100_SW_2	A host safety application shall register with ISI for using any of the services provided by ISI. Host SW shall implement watchdog monitoring of periodic DTI_sync message from ISI	CoU_SWARCH_04 CoU_SWARCH_06A
AoU_SCB100_SW_3	The user of SCB100 shall guarantee that configured PST parameter shall not be greater than 21sec.	CoU_SWARCH_06B
AoU_SCB100_SW_4	In a safety control loop, SW shall send periodic diagnostic messages early enough to Intel® Safety Island so that it has required time to process the snapshots/results and in event of fault drive NOK within **"EHL reaction time budget"**.	CoU_SWARCH_07

8 Safety Analysis Results

8.1. FMEDA Report

Table 24 and Table 25 shows the FMEDA result of SCB100. For more details, please contact NexCOBOT to acquire the FMEDA report for SCB100.

For 1oo1 system: $PFH_G = \lambda_{DU}$

For 1oo2 system: $PFH_G = 2\big((1-\beta)\lambda_{DD} + (1-\beta)\lambda_{DU}\big)(1-\beta)\lambda_{DU}t_{CE} + \beta\lambda_{DU}$

where $t_{CE} = \frac{\lambda_{DU}}{\lambda_D}\left(\frac{T_1}{2} + \mathrm{MRT}\right) + \frac{\lambda_{DD}}{\lambda_D}\mathrm{MTTR}$

For SCB100 FMEDA SIL2 HFT=0 Results:

$$\begin{aligned}\mathrm{PFH\_total} = {} & PFH\_CPU\ (using\ 1oo1\ formula\ from\ Intel) \\ & + PFH\_power\ (using\ 1oo1\ formula) \\ & + PFH\_DDR\ (using\ 1oo1\ formula) \\ & + PFH\_EMMC\ (using\ 1oo1\ formula) \\ & + 12\ x\ PFH\_DI\ (using\ 1oo2\ formula) \\ & + 8\ x\ PFH\_DO\ (using\ 1oo2\ formula) \\ & + PFH\_NVRAM\ (using\ 1oo1\ formula) \\ & + PFH\_clock\ (using\ 1oo1\ formula)\end{aligned}$$

Table 24. SCB100 FMEDA SIL2 HFT=0 Results

SIL2 HFT=0	SCB100 with Intel Atom® x6427FE
DC	99.39%
SFF	99.68%
PFH (Failures/Hour)	6.103E-08

* With 12 inputs and 4 outputs

For SCB100 FMEDA Cat3 PL=d Results:

$$\text{PFH\_total} = PFH\_CPU\ (using\ 1oo2\ formula\ from\ Intel) + PFH\_power\ (using\ 1oo1\ formula) + PFH\_DDR\ (using\ 1oo1\ formula) + PFH\_EMMC\ (using\ 1oo1\ formula) + 12\ x\ PFH\_DI\ (using\ 1oo2\ formula) + 8\ x\ PFH\_DO\ (using\ 1oo2\ formula) + PFH\_NVRAM\ (using\ 1oo1\ formula) + PFH\_clock\ (using\ 1oo1\ formula)$$

Table 25. SCB100 FMEDA Cat3 PL=d Results

Cat.3 PL=d	SCB100 with Intel Atom® x6427FE	Units
PFH_d (Permanent and Transient)	1.30E-08	Failures [hr^{-1}]
DC_{avg}	99.43	%
$MTTF_d$ (Permanent Only)	60.22	years
$MTTF_d$ (Permanent and Transient)	15.54	years
CCF Score	95 (> 65)	N/A

* With 12 inputs and 4 outputs

8.2. External DDR4 memory

Due to external DDR4 memory is out of the scope of SCB100, the failure rate of external DDR4 memory shall be additionally considered by the user.

Appendix A SCB100 Specification

Table 26. SCB100 Specification

Part	Item		Specification
Hardware	CPU	Safety Related	Intel Atom® x6427FE, 4 Cores 1.9GHz
	RAM	Safety Related	2x DDR4 SO-DIMM, support up to 32GB
	Storage	Safety Related	On board 64GB EMMC
		-	SATA Interface
	Mini-PCIe	Black Channel	1 x miniPCIe
	COM Port	Black Channel	2 x RS232/422/485 with Auto flow control
	EtherCAT	Black Channel	1 x EtherCAT slave (2 x RJ45 Ports)
	Ethernet	Black Channel	1 x I225 GbE LAN, 3 x GbE LAN
	Digital Inputs	Safety Related	12 inputs, 24 VDC SELV/PELV, 2~15mA, H: 11-30VDC L: 0-5VDC
	Digital Outputs	Safety Related	4 outputs, 24 VDC SELV/PELV, 0.5A of each channel, 2A of total DO channel ON: output voltage > 18VDC, OFF: output voltage < 3VDC
	Power	Safety Related	AT/ATX mode (by jumper setting default-AT) 24 VDC SELV/PELV -15% ~ +20%, acc. to IEC 61131-2, 4-pin power connector for DC input
	USB		2 x USB 3.0, 4 x USB 2.0
	Display		1 x HDMI
	Dimension		Mini-ITX (17cm x 17cm)
	Environment		Operating: -20~60℃,Storage: -40~85℃, Relative Humidity: 90%
	Vibration		Comply with IEC 61131-2 Sinusoidal vibration conditions Displacement: 3,5 mm constant displacement, 5 ≤ f < 8,4 Hz

			Acceleration: 10 m/s^2 (1 g) constant acceleration, 8,4 ≤ f ≤ 150 Hz
	Shock		Comply with IEC 61131-2 150 m/s^2 (15 g), 11 ms, half-sine, in each of 3 mutually perpendicular axes
	EMC		Comply with IEC 61326-3-1, IEC 61131-2
Software	FW	Intel Elkhart Lake FWs	SIL 3, Pre-loaded to SCB100
	BIOS	Intel Slim Bootloader	Modified version for SCB100, Pre-loaded to SCB100
		Intel PreOS Checker	SIL 3, Pre-loaded to SCB100
	APIs	Intel Elkhart Lake Safety APIs	SIL 3, Source Code available Note: Requires NDA with Intel to download source code
Documents		SCB100 Safety Manual SCB100 Failure Mode and Effects Analysis (FMEDA) Report	
Ordering Information		SCB100 P/N: 10Q00010007X0 (1 pcs) 10Q00010008X0 (10 pcs)	
Note: SCB100 does not have an enclosure, therefore the user of SCB100 shall implement the ingress protection measures at application level.			

Appendix B SCB100 Bring up

B.1 SCB100 Package Content

The SCB100 package includes the hardware components listed in Table 27 below. Please ensure that the package is complete and inspect it for any damage that may have occurred during shipment.

Table 27. Included in SCB100 package

NO.	Description	Qty
1	SCB100 Main board	1
2	SCB100 I/O Board	1
3	Copper post long fei	2
4	Round head screw W/Spring + flat washer long fei :P3x7L	4
5	RTC Battery (3V)	1
6	DC power-in cable (with Power in connector, refer to B.2.2 Power In Connector)	1

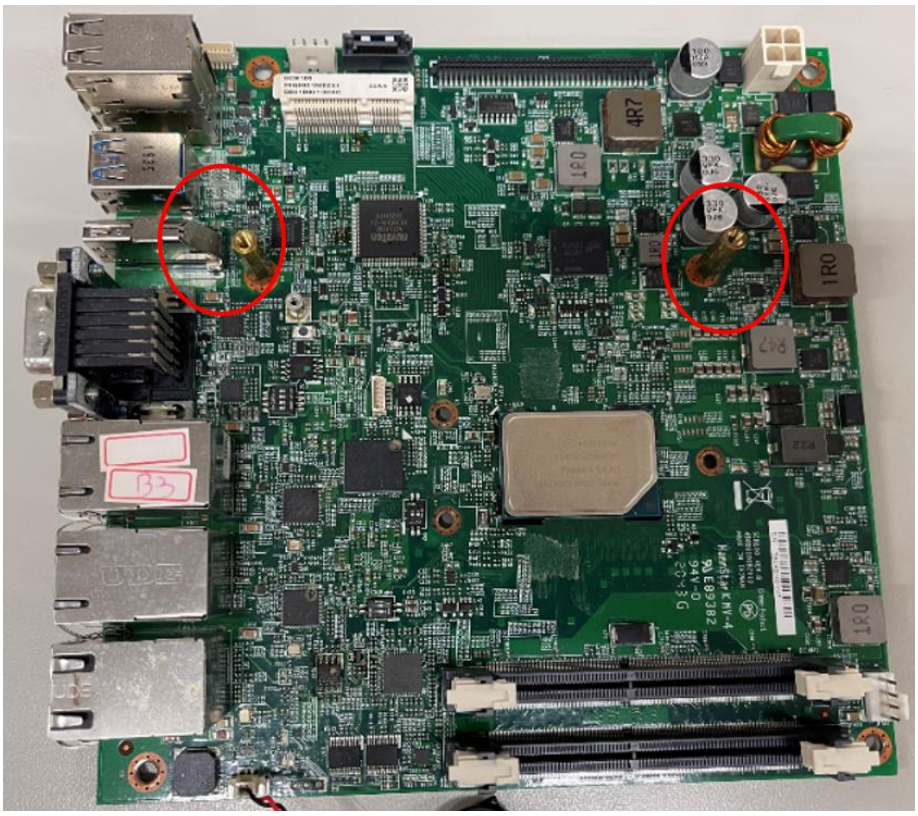


Figure 15. Copper post long fei

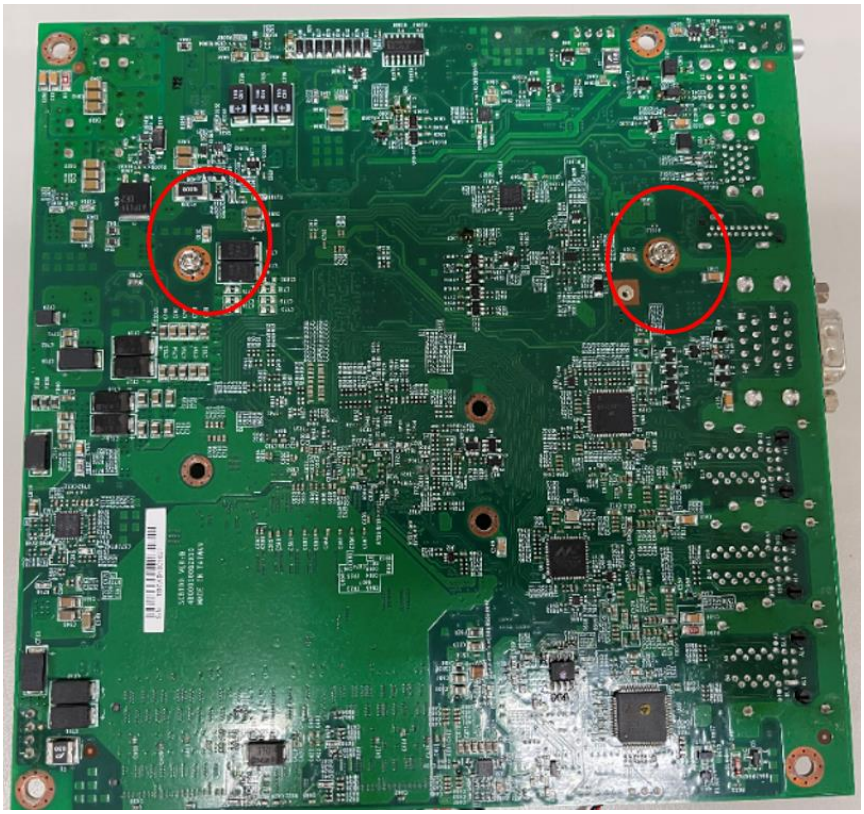


Figure 16. Round head screw W/Spring + flat washer long fei :P3x7L - 1

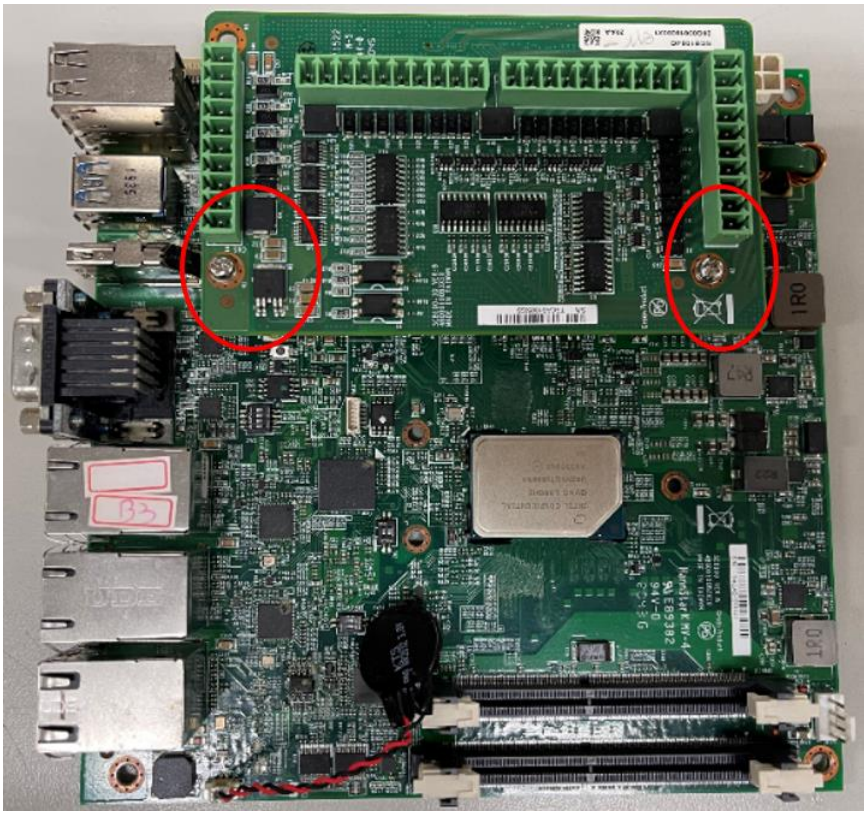


Figure 17. Round head screw W/Spring + flat washer long fei :P3x7L - 1

Table 28. **IS NOT** included in SCB100 package

NO.	Item	Reference Model/Specification	Qty
1	DC IN 3 Pin Connector	Phoenix contact: MSTB 2,5/ 3-STF-5,08 https://www.phoenixcontact.com/online/portal/us?uri=pxc-oc-itemdetail:pid=1777992&library=usen&tab=1	1
2	DDR4 4GB RAM	Innodisk 4GB DDR4 2400 SODIMM or Transcend 4GB DDR4 2400 SODIMM	1
3	Power adapter	AC Input: 100~240V, 1.5A, 50~60Hz DC output: 24V, 2.5A	1

B.2 Internal Connector Definition

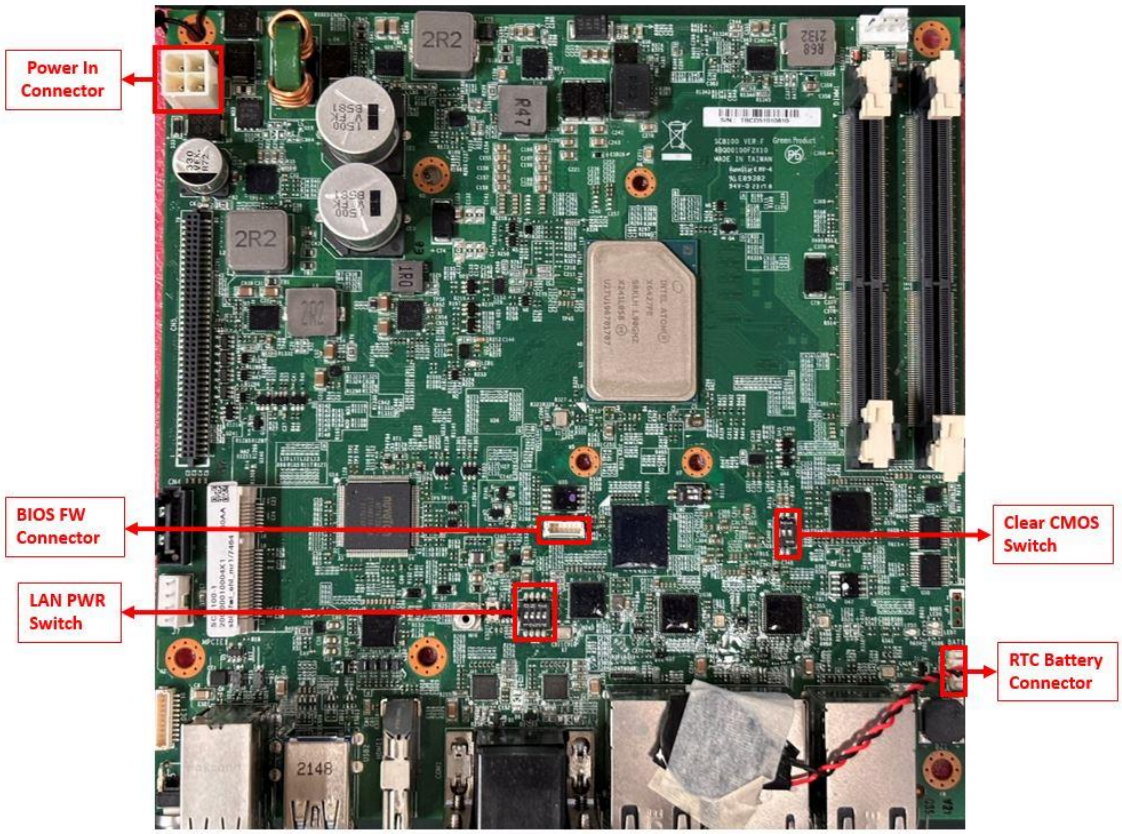


Figure 18. Internal Connector location

B.2.1 RTC Battery Connector

1. Location and Size: BAT1 / 1 X 2 = 2 Pin , 1.25mm , 180°, MALE,SMD.
2. Manufacturing name and Part number: ANYTRONIC:1812022S02A0N6T-1HF-R.
3. Contact and Plated: Copper Alloy , Tin plated.

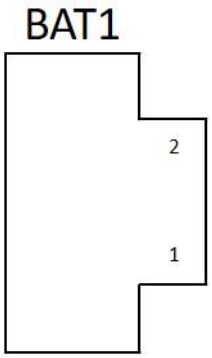


Figure 19. RTC Battery Connector Port Mapping

Table 29. RTC Battery Connector Pin Definition

Pin	Definition	Description
1	GND	GND(Black)
2	3V_BAT1	RTC Power (Red)

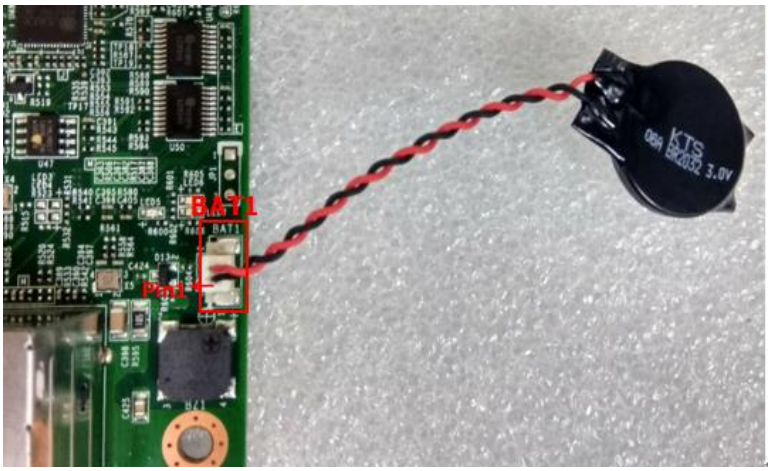


Figure 20. RTC Battery Sample

B.2.2 Power In Connector

1. Location and Size: JDC1 / 4 Pin , 180°,MALE,DIP.
2. Manufacturing name and Part number: ANYTRONIC:25101A0400B0-3RF.
3. Contact and Plated: Copper alloy, Tin plated.

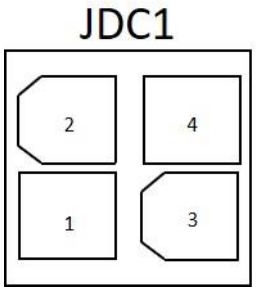


Figure 21. Power In Connector Port Mapping

Table 30. Power In Connector Pin Definition

Pin	Definition	Description
1	GND	GND

2	GND	GND
3	+24V	DC 24V Power IN
4	+24V	

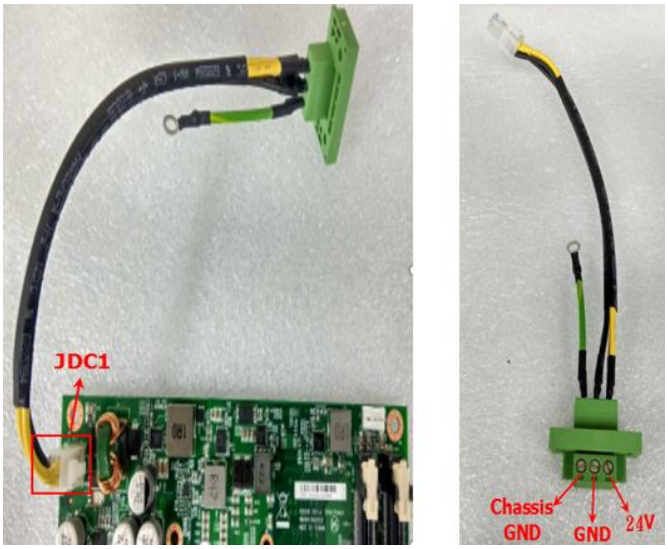


Figure 22. Example of DC power-in cable wired to the Power In Connector.

Note: The power DC power-in cable sample is included in SCB100 package.

B.2.3 Clear CMOS Switch

1. Location and Size: SW3 / 2 X 2 = 4 Pin , 1.27mm ,SMD.
2. Manufacturing name and Part number: HCH:HPS602-E.
3. Contact and Plated: Copper Alloy, Gold plated.

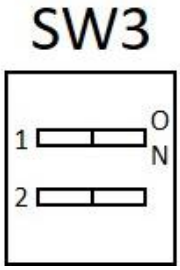


Figure 23. Clear CMOS Switch Port Mapping

Table 31. Clear CMOS Switch Default Setting

CLRCMOS

*OFF	Normal
ON	Clear CMOS

B.2.4 LAN PWR Switch

1. Location and Size: SW5 / 2 X 4 = 8 Pin , 1.27mm ,SMD.
2. Manufacturing name and Part number: HCH:HPS604-E.
3. Contact and Plated: Copper Alloy, Gold plated.

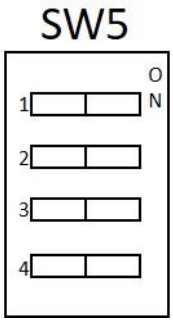


Figure 24. LAN PWR Switch Port Mapping

Table 32. LAN PWR Connector Pin Definition

LAN PWR Switch	
*OFF	Disable
ON	Enable

Note: Enable/Disable LAN/PHY Power by safety control pin.

B.2.5 BIOS FW Connector

1. Location and Size: JFW1 / 1 X 6 = 6 Pin, 1.0mm ,180°, Male, SMD
2. Manufacturing name and Part number: ACES:50228-0067N-003
3. Contact and Plated: Copper Alloy, Tin plated

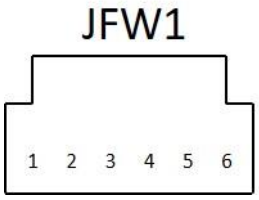


Figure 25. BIOS FW Connector Port Mapping

Table 33. LAN PWR Connector Pin Definition

Pin	Definition	Description
1	VSPI	3.3V Power
2	GND	GND
3	BIOSSPICSL0	Chip select
4	BIOSSPICLK	Clock
5	BIOSSPISO	MISO
6	BIOSSPISI	MOSI

B.2.6 DIO Connector (I/O Board)

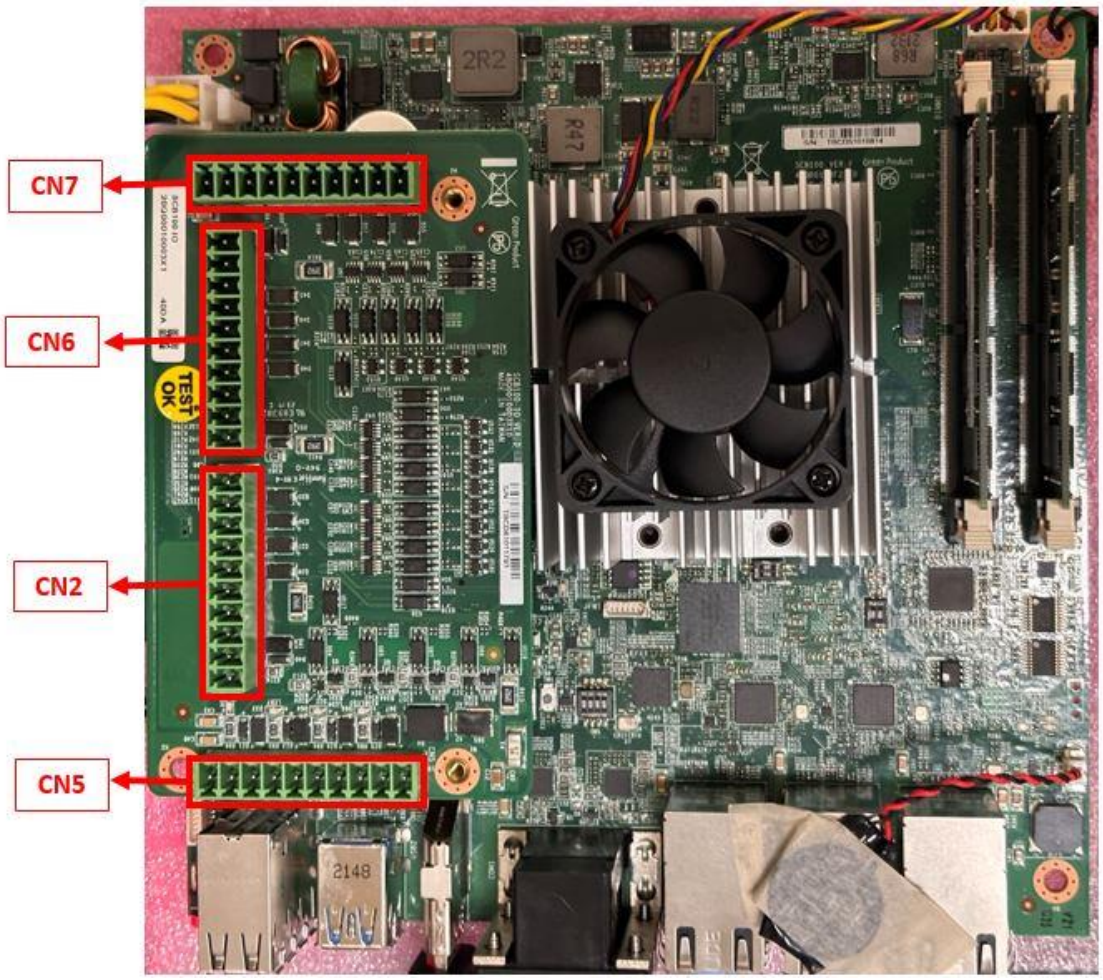


Figure 26. DIO Connector location

1. Location and Size:
   1.1 (DI1-DI4)CN2 / 1X10=10 Pin , 3.81mm,180°, FEMALE, DIP.
   1.2 (DI5-DI8)CN6 / 1X10=10 Pin , 3.81mm,180°, FEMALE, DIP.
   1.3 (DI9-DI12)CN7 / 1X10=10 Pin , 3.81mm,180°, FEMALE, DIP.
   1.4 (DO1-DO4)CN5 / 1X10=10 Pin , 3.81mm,180°, FEMALE, DIP.
2. Manufacturing name and Part number: PHOENIX CONTACT:1803507.
3. Contact and Plated: Copper alloy ,Tin plated.

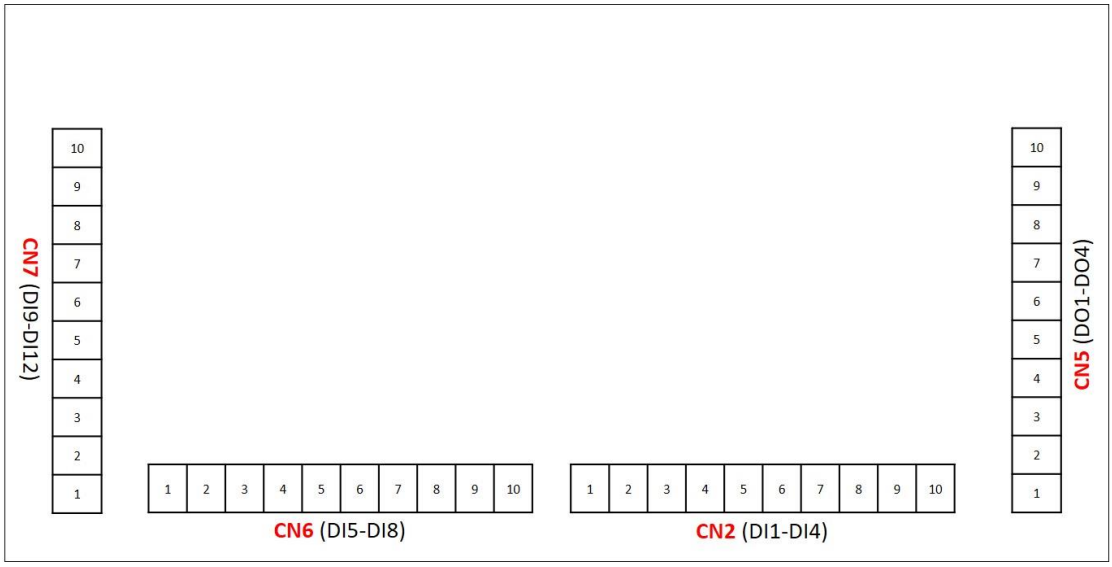


Figure 27. DIO Connector in number location

Table 34. CN2 (DI1-DI4) Connector Pin Definition

Pin	Definition	Description
1	DI1+	Digital input 1+
2	DI1-	Digital input 1-
3	DI2+	Digital input 2+
4	DI2-	Digital input 2-
5	DI3+	Digital input 3+
6	DI3-	Digital input 3-
7	DI4+	Digital input 4+
8	DI4-	Digital input 4-
9	DI_24VIN	Digital input 24V IN
10	DI_GND	Digital input GND

Table 35. CN6 (DI5-DI8) Connector Pin Definition

Pin	Definition	Description
1	DI5+	Digital input 5+
2	DI5-	Digital input 5-
3	DI6+	Digital input 6+
4	DI6-	Digital input 6-

5	DI7+	Digital input 7+
6	DI7-	Digital input 7-
7	DI8+	Digital input 8+
8	DI8-	Digital input 8-
9	DI_24VIN	Digital input 24V IN
10	DI_GND	Digital input GND

Table 36. CN7 (DI9-DI12) Connector Pin Definition

Pin	Definition	Description
1	DI9+	Digital input 9+
2	DI9-	Digital input 9-
3	DI10+	Digital input 10+
4	DI10-	Digital input 10-
5	DI11+	Digital input 11+
6	DI11-	Digital input 11-
7	DI12+	Digital input 12+
8	DI12-	Digital input 12-
9	DI_24VIN	Digital input 24V IN
10	DI_GND	Digital input GND

Table 37. CN5 (DO1-DO4) Connector Pin Definition

Pin	Definition	Description
1	DO1+	Digital Output 1+
2	DO1-	Digital Output 1-
3	DO2+	Digital Output 2+
4	DO2-	Digital Output 2-
5	DO3+	Digital Output 3+
6	DO3-	Digital Output 3-
7	DO4+	Digital Output 4+
8	DO4-	Digital Output 4-

9	DO_24VIN	Digital Output 24V IN
10	DO_GND	Digital Output GND

B.3 Power On SCB100

B.3.1 Pre-requirements

The following ingredients are required to power on the SCB100:

1. Power adaptor and connector (not supplied by NexCOBOT, please refer to Table 28).
2. USB type Keyboard and Mouse (not supplied by NexCOBOT, please refer to Table 28).
3. SATA SSD or USB with Operating System installed (Please contact Safety OS vendor to obtain OS image, or contact NexCOBOT for more advice on Safety OS vendors).
4. External display and cable (i.e., HDMI monitor, not supplied by NexCOBOT).

B.3.2 Powering up the SCB100

Refer to Figure 32 for connector and component locations.

1. Install memory card in DIMM socket, installation method can refer to below step.

Step 1. The DIMM socket has both retaining clips.

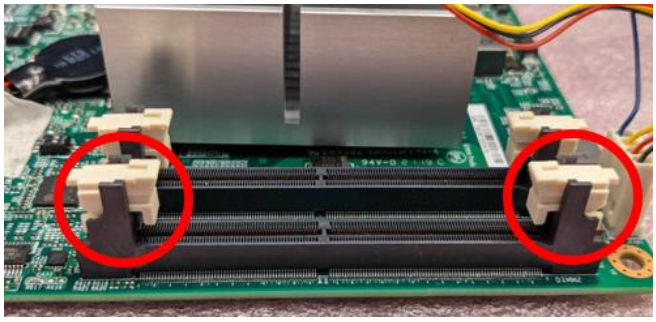


Figure 28. Install memory card step one

Step 2. The retaining clips shall be open like below figure and make sure you align your memory in the correct direction during RAM installation.

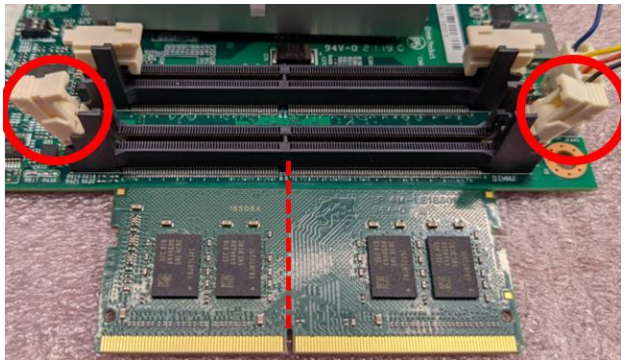


Figure 29. Install memory card step two

Step 3. Holding your memory card, apply equal downward pressure on both sides and push it into the DIMM slot.

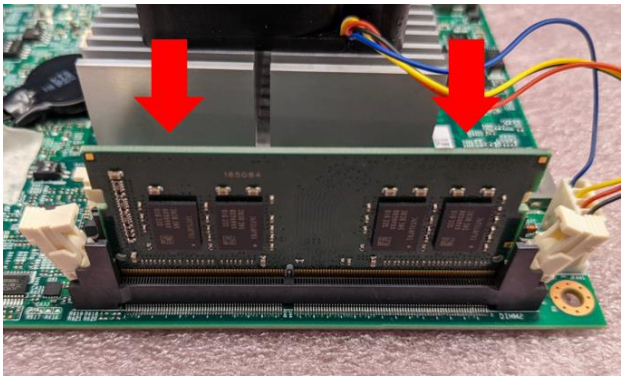


Figure 30. Install memory card step three

Step 4. Both retaining clips will snap into place once the memory card has been fully inserted.

Figure 31. Install memory card step four

2. Connect to HDMI1 monitor for display output.
3. SCB100 I/O board installed on SCB100 board before shipment.

4. Connect SATA SSD or USB drive with OS installed to SATA Conn or USB port.
5. Connect USB mouse/Keyboard to USB port.
6. Connect power adaptor (AC brick) to power jack JDC1 (The SCB100 shall boot up automatically without pressing power button).
7. The system boots up and is ready for use.

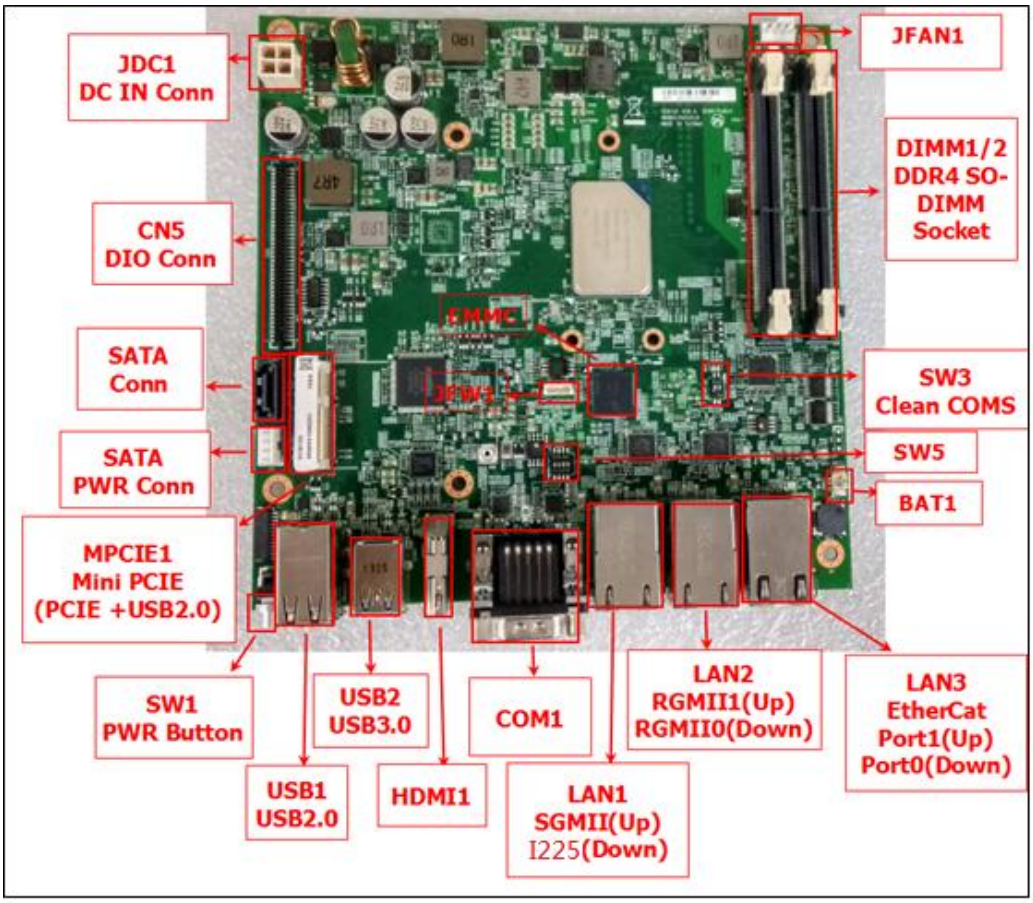


Figure 32. SCB100 Sample Function Top View

Appendix C Hardware & Software interface

For more details, please contact NexCOBOT to get the file [6].

C.1 GPIO pins

Table 38. SCB100 GPIO Pin Status

GPIO function	Status address in register	Status
GPI	Bit: 1	0: no Input 1: has input
GPO	Bit: 0	0: no Output 1: has Output

C.1.1 Digital Input related GPIO pin register

Table 39. Digital Input related GPIO pin register

GPIO Function Name	Register Address	GPIO Type
GPIA_1	fd6e09a0	GPI
GPIA_2	fd6e09b0	GPI
GPIA_3	fd6e09c0	GPI
GPIA_4	fd6e0b10	GPI
GPIA_5	fd6e09d0	GPI
GPIA_6	fd6e09e0	GPI
GPIA_7	fd6e09f0	GPI
GPIA_8	fd6e0a00	GPI
GPIA_9	fd6d0a10	GPI
GPIA_10	fd6d0a20	GPI
GPIA_11	fd6d0a30	GPI
GPIA_12	fd6d0a40	GPI
GPIB_1	fd6d0840	GPI
GPIB_2	fd6d0850	GPI

GPIB_3	fd6d0860	GPI
GPIB_4	fd6d0870	GPI
GPIB_5	fd6e0930	GPI
GPIB_6	fd6e0940	GPI
GPIB_7	fd6e0960	GPI
GPIB_8	fd6e0970	GPI
GPIB_9	fd6a07f0	GPI
GPIB_10	fd6a0840	GPI
GPIB_11	fd6a0850	GPI
GPIB_12	fd6a0860	GPI
(Test Pulse Control) TPC_1	fd6d0a60	GPO
TPC_2	fd6d0a70	GPO
TPC_3	fd6d0a80	GPO
TPC_4	fd6d0a90	GPO
TPC_5	fd6e0a10	GPO
TPC_6	fd6e0a20	GPO
TPC_7	fd6e0a30	GPO
TPC_8	fd6e0a40	GPO
TPC_9	fd6d0aa0	GPO
TPC_10	fd6d08c0	GPO
TPC_11	fd6d08d0	GPO
TPC_12	fd6d08f0	GPO

C.1.2 Digital output related GPIO pin register

Table 40. Digital output related GPIO pin register

GPIO Function Name	Register Address	GPIO Type
GPOA_1	fd6e07f0	GPO
GPOA_2	fd6e0800	GPO
GPOA_3	fd6e0810	GPO
GPOA_4	fd6e0830	GPO
GPOB_1	fd6a07b0	GPO
GPOB_2	fd6a07c0	GPO
GPOB_3	fd6a07d0	GPO
GPOB_4	fd6a07e0	GPO
(DO Monitor) DOM_1	fd6e0740	GPI
DOM_2	fd6e0750	GPI
DOM_3	fd6e0760	GPI
DOM_4	fd6e0770	GPI

C.1.3 Other diagnostic related GPIO pin register

Table 41. Other diagnostic related GPIO pin register

GPIO Function Name	Register Address	GPIO Type	Effective bit
Voltage Monitor Error	fd6d0980	GPI	1
Safety Control Monitor	fd6d09a0	GPI	1
GPO Voltage Monitor	fd6a0bb0	GPI	1
GPIA Voltage Monitor	fd6a0930	GPI	1
GPIB Voltage Monitor	fd6a0940	GPI	1
GPIC Voltage Monitor	fd6a0950	GPI	1

When the diagnostic measures of Power which are described in 5.2 detected failures of Power, SCB100 will enter safe state. The user SW applications can read the status of「Voltage Monitor Error」GPI pin about Power diagnostic measures.

Table 42. Voltage Monitor Error GPIO pin

GPIO Function Name	Input value	
	No error	Error
Voltage Monitor Error	1	0

When SCB100 in safe state, which means Logic function in Figure 3 output a safety control signal to SCB100 to let SCB100 enter safe state. The user SW applications can read the status of「Safety Control Monitor」GPI pin about safe state.

Table 43. Safety Control Monitor GPIO pin

GPIO Function Name	Input value	
	In safe state	Not in safe state
Safety Control Monitor	1	0

The user software application can read the 「GPIO pin Input Power Monitor」 GPIO pin to verify if the GPIO 24V input power supply is operating normally.

Table 44. GPIO pin Input Power Monitor

GPIO Function Name	Input value	
	In safe state	Not in safe state
GPO Voltage Monitor	1	0
GPIA Voltage Monitor	1	0
GPIB Voltage Monitor	1	0
GPIC Voltage Monitor	1	0

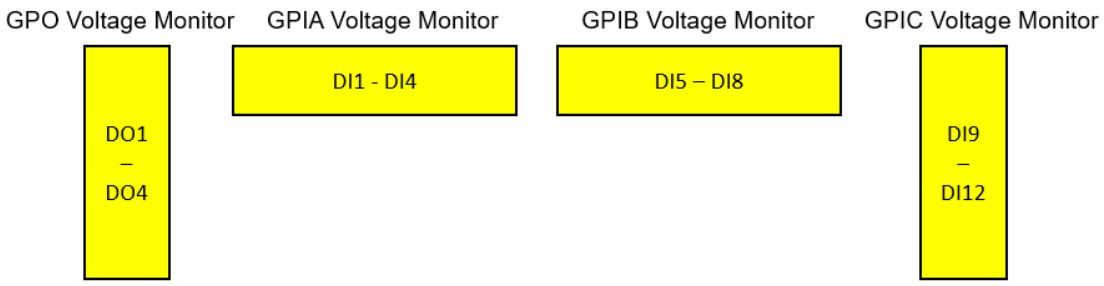


Figure 33. Mapping description for GPIO Input Power Monitor

C.2 Ethernet

Table 45. Ethernet HW&SW Interface

NO.	Ethernet controller	Communication BUS to CPU	
#0	Intel I225	PCIE	HSIO Lane4
#1	GbE controller in PCH(PSE0)	RGMII	
#2	GbE controller in PCH(PSE1)	RGMII	
#3	GbE controller in PCH	SGMII	HSIO Lane8

C.3 EtherCAT

Table 46. EtherCAT HW&SW Interface

EtherCAT Salve Controller(ESC)	PCIE to ESC Controller	Communication BUS to CPU	
AX58100	AX99100	PCIE	HSIO Lane5

C.4 COM port

Table 47. COM port HW&SW Interface

NO.	Super I/O	Communication BUS to CPU	
COM1	F81439AN	eSPI	RS232/422/485
COM2			RS232/422/485

C.5 Mini-PCIe slot

Table 48. Mini-PCIe HW&SW Interface

Item	Communication BUS to CPU	
PCIE	PCIE	HSIO Lane
USB2.0	USB2.0	USB 2.0 port 8

C.6 USB

Table 49. USB HW&SW Interface

Item	Communication BUS to CPU	
USB3.0#1	USB3.0	USB 3.0 pair 0
USB3.0#2	USB3.0	USB 3.0 pair 1
USB2.0#1	USB2.0	USB 2.0 port 2
USB2.0#2	USB2.0	USB 2.0 port 3
USB2.0#3	USB2.0	USB 2.0 port 4
USB2.0#4	USB2.0	USB 2.0 port 5

Appendix D Environmental and EMC tests

Note:

Due to the user of SCB100 needs to design the enclosure for it, the environmental tests and EMC tests shall be repeated by the user on the final complete safety-related programmable electronic system.

D.1 Environmental tests

IEC 61131-2 (Environment related)	
Basic Standard	Test Value
Dry-heat Immunity test (IEC 60068-2-2)	Temperature: 60°C Duration: 16 hours
Cold Immunity test (IEC 60068-2-1)	Temperature: 0°C Duration: 16 hours
Dry-heat Withstand test (IEC 60068-2-2)	Temperature: 70°C Duration: 16 hours
Mechanical shock test (IEC 60068-2-27)	Pulse shape: Half-sine Acceleration: 150 m/s^2 Pulse duration: 11ms Shock direction: 6 faces NO. of shock: 3 shocks/ axis (total 18 shocks)
Sinusoidal vibration test (IEC 60068-2-6)	Waveform: Sinusoidal Frequency: (5~150) Hz Displacement: 3.5mm (5Hz~8.4Hz) Acceleration: 10 m/s^2 (8.4Hz~150Hz) Sweep rate: 1 octave/ minute Direction: X,Y,Z Axes Duration: 10 sweep cycles/ axis
Cold Withstand test (IEC 60068-2-1)	Temperature: -25°C Duration: 16 hours
Cyclic damp-heat Withstand test	Temperature: 55°C

(IEC 60068-2-30)	Test Humidity: 95% Duration: 24 hours
Change of temperature Immunity test (IEC 60068-2-14)	Minimum Ambient temperature:0°C Maximum Ambient temperature:60°C Temperature venation speed:3K/min±0.6K/min Exposure time at each temperature:3 h ± 30 min Number of cycles:2
Cyclic damp-heat Immunity test (IEC 60068-2-78)	Temperature: 30°C Test Humidity: 93% Duration: 16 hours
Change of temperature Withstand test (IEC 60068-2-14)	Minimum Ambient temperature:-25°C Maximum Ambient temperature:70°C Transport time: Less than 3 min Exposure time at each temperature:3 h ± 30 min Number of cycles:5 Conditioning: Power supply unconnected

D.2 EMC tests

Table 50. IEC 61326-3-1 tests

IEC 61326-3-1		
Basic Standard	Level	Criteria
IEC 61000-4-2 (ESD)	Air discharge:±8kV Contact discharge:±6kV	DS*1
IEC 61000-4-3 (RS)	Frequency:80 MHz ~ 1GHz Level:20V/m, 80% AM Frequency:1.4GHz~2GHz	DS*1

	Level:10V/m, 80% AM Frequency:2GHz~6GHz Level:3V/m, 80% AM	
IEC 61000-4-4 (EFT)	DC Power: (L/N) ±3kV HDMI/Ethernet/COM/EtherCAT/DIO: ±2kV	DS*1
IEC 61000-4-5 (Surge)	DC Power: ±1kV(line to line) ±2kV(line to earth or ground) Signal ports: Ethernet/RS485/ RS422/EtherCAT/DIO ±2kV	DS*1
IEC 61000-4-6 (CS)	DC Power/IO Power HDMI/Ethernet/EtherCAT/COM/DIO Frequency:0.15MHz ~ 80MHz Level:10 V,80% (1kHz 80% AM)	DS*1
IEC 61000-4-8 (PFMF)	30 A/m	DS*1
IEC 61000-4-16 (Conducted common mode voltage)	1 V to 10 V, 20 dB/Decade (1,5 kHz to 15 kHz) 10 V (15 kHz to 150 kHz) 10 V (DC, 16 2/3 Hz, 50/60 Hz and 150/180 Hz) 100 V short duration (1 s, DC, 16 2/3 Hz and 50/60 Hz)	DS*1
IEC 61000-4-29 (mode voltage)	Voltage dips 40 % UT for 10 ms Voltage interruptions 0 % UT for 20 ms	DS*1

Note:

“DS*1” means no loss of the safety function and permanently provided that a safe state of the machine is maintained.

"DS*2" means the safety function may be disturbed temporarily, and permanently provided that a safe state of the machine is maintained or achieved before a hazard can occur.

Table 51. IEC 61131-2 tests (EMC related)

IEC 61131-2 (EMC related)		
Basic Standard	Level	Criteria
Conducted Emission (IEC 61000-6-4:2018)	Same as IEC 61000-6-4 (see Table 52)	Class A limit
Conducted Emission at Telecommunication Port (ISN) (IEC 61000-6-4:2018)	Same as IEC 61000-6-4 (see Table 52)	Class A limit
Radiated Emissions Below 1GHz (IEC 61000-6-4:2018)	Same as IEC 61000-6-4 (see Table 52)	Class A limit
Radiated Emissions Above 1GHz (IEC 61000-6-4:2018)	Same as IEC 61000-6-4 (see Table 52)	Class A limit
IEC 61000-4-2 (ESD)	Air discharge:±8kV Contact discharge:±4kV	A
IEC 61000-4-3 (RS)	Frequency:80 MHz ~ 1GHz Level:10V/m, 80% AM Frequency:1.4GHz~2GHz Level:3V/m, 80% AM Frequency:2GHz~2.7GHz Level:3V/m, 80% AM Frequency:2.7GHz~6GHz Level:3V/m, 80% AM	A
IEC 61000-4-4 (EFT)	DC Power:	A

	±2kV HDMI/Ethernet/COM/EtherCAT/DIO: ±1kV	
IEC 61000-4-5 (Surge)	DC Power: ±0.5kV(line to line) ±0.5kV(line to earth or ground) Signal ports: Ethernet/RS485/RS455/ EtherCAT/DIO ±1kV	A
IEC 61000-4-6 (CS)	DC Power/IO Power HDMI/Ethernet/EtherCAT/COM Frequency:0.15MHz ~ 80MHz Level:10 V,80% AM	A
IEC 61000-4-8 (PFMF)	60 Hz, 30A/M 50Hz, 30A/M	A

Note:

“A” means the EUT continued to operate as intended. No degradation of performance or loss of function was allowed below a performance level specified by the manufacturer, when the EUT was used as intended.

Table 52. IEC 61000-6-2 / IEC 61000-6-4 tests

IEC 61000-6-2 / IEC 61000-6-4		
Basic Standard	Level	Criteria
Conducted Emission (IEC 61000-6-4:2018)	Frequency:0.15 ~ 0.5 MHz Limit: Quasi-peak 89dBuV Average 76dBuV	Class A limit

	Frequency:0.5 ~ 30 MHz Limit: Quasi-peak 83dBuV Average 70dBuV	
Conducted Emission at Telecommunication Port (ISN) (IEC 61000-6-4:2018)	Frequency:0.15 ~ 0.5 MHz Limit: Quasi-peak 97~87dBuV Average 84~74dBuV Frequency:0.5 ~ 30 MHz Limit: Quasi-peak 87dBuV Average 74dBuV	Class A limit
Radiated Emissions Below 1GHz (IEC 61000-6-4:2018)	Frequency:30 ~ 230 MHz Limit: Quasi-peak 40 dBuV/m @10m Frequency:230 ~ 1GHz Limit: Quasi-peak 47 dBuV/m @10m	Class A limit
Radiated Emissions Above 1GHz (IEC 61000-6-4:2018)	Frequency:1 ~ 3GHz Limit: Peak 76dBuV/m @3m Average 56dBuV/m @3m Frequency:3 ~ 6GHz Limit: Peak 80dBuV/m @3m Average 60dBuV/m @3m	Class A limit
IEC 61000-4-2 (ESD)	Air discharge:±8kV	A

	Contact discharge:±4kV	
IEC 61000-4-3 (RS)	Frequency:80 MHz ~ 1GHz Level:10V/m, 80% AM (1kHz) Frequency:1.4GHz~6GHz Level:3V/m, 80% AM	A
IEC 61000-4-4 (EFT)	DC Power: ±1kV HDMI/Ethernet/COM/EtherCAT: ±1kV	A
IEC 61000-4-5 (Surge)	DC Power: ±0.5kV(line to line) ±1kV(line to earth or ground) Signal ports: Ethernet/COM-RS484, RS-422/EtherCAT ±1kV	A
IEC 61000-4-6 (CS)	DC Power/IO Power HDMI/Ethernet/EtherCAT/COM Frequency:0.15MHz ~ 80MHz Level:10 V,80% AM	A
IEC 61000-4-8 (PFMF)	30 A/m	A

Note:

“A” means the EUT continued to operate as intended. No degradation of performance or loss of function was allowed below a performance level specified by the manufacturer, when the EUT was used as intended.